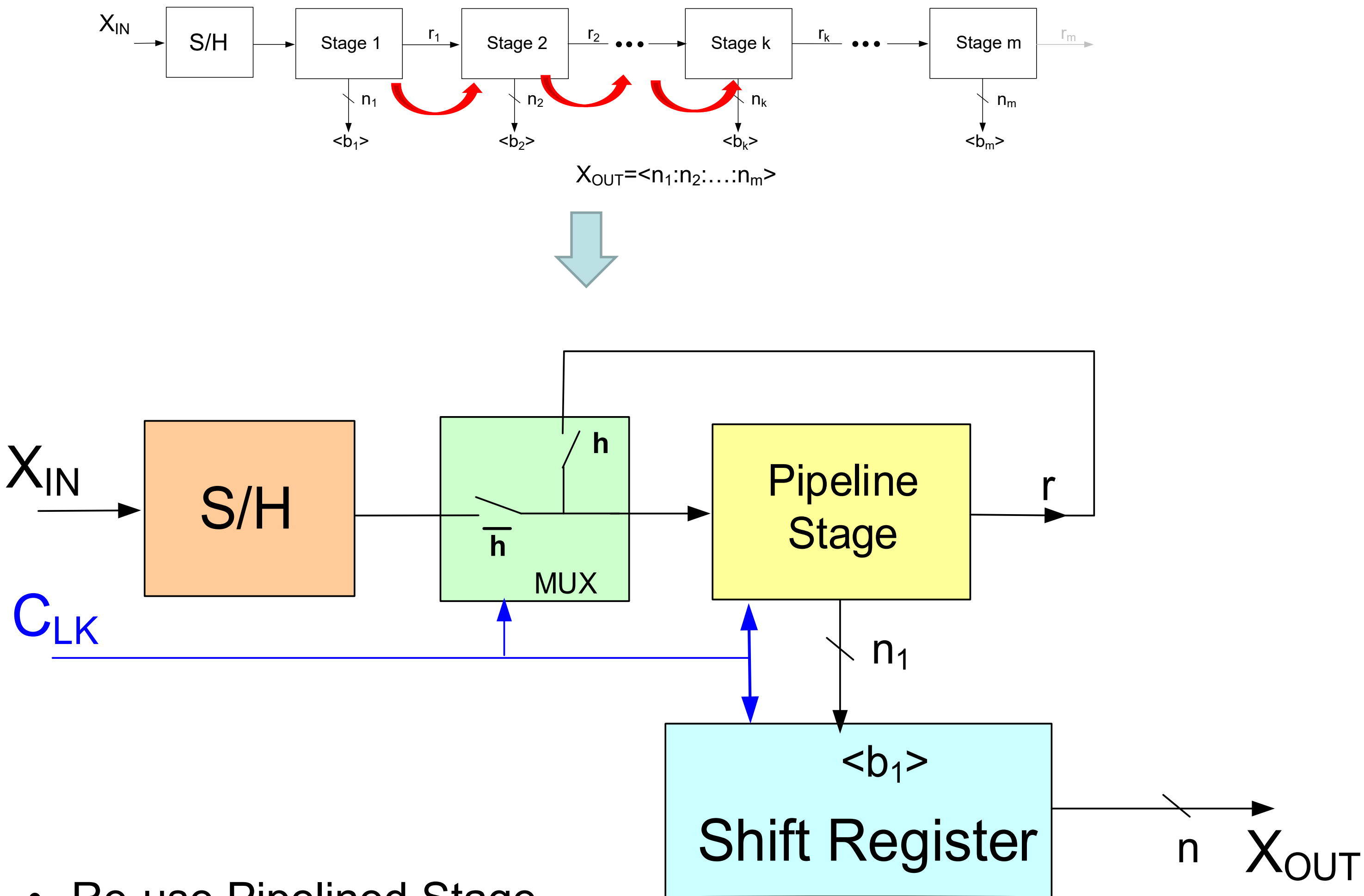
EE 435

Lecture 38

Data Converters

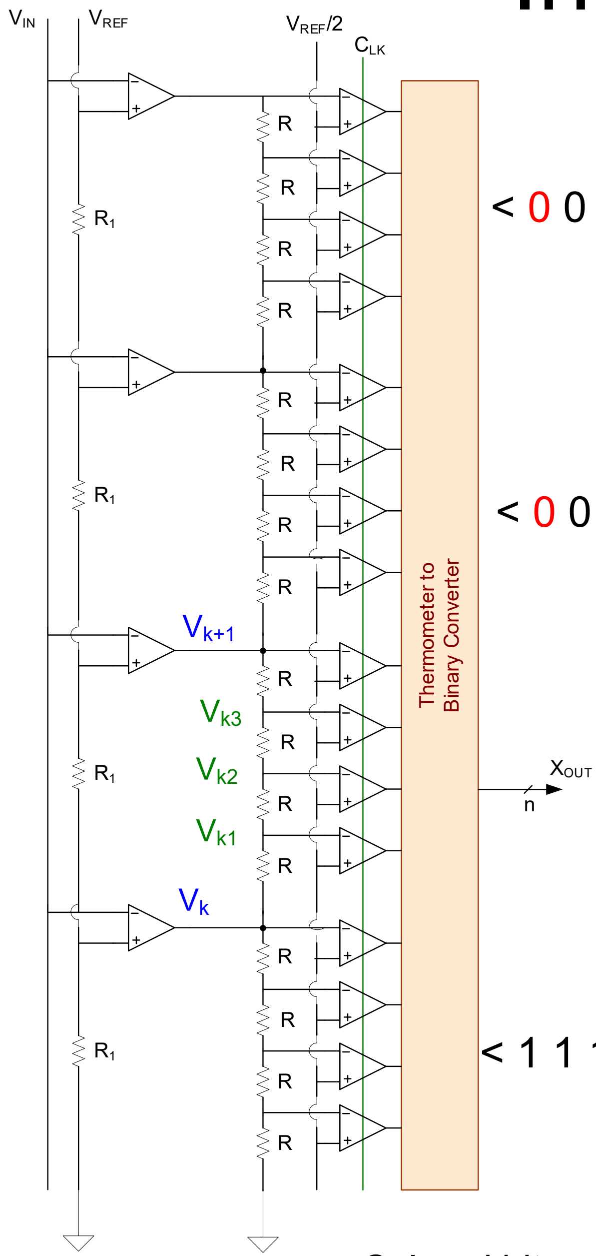
- Noise
- Statistical Characterization

Cyclic (Algorithmic) ADC



- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases

Interpolating ADC

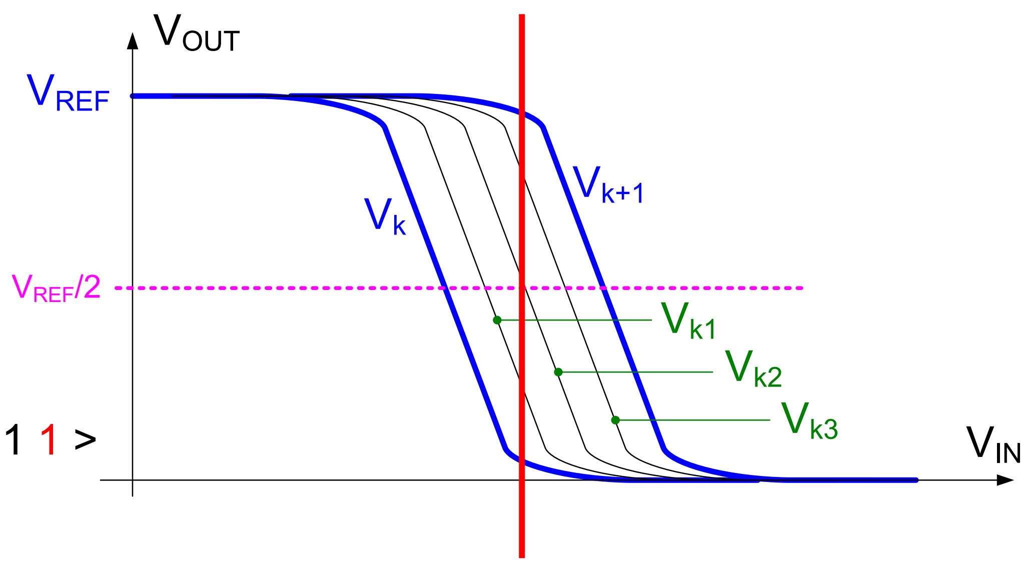


< 0 0 0 0 0 >

< 0 0 0 0 0 >

< 1 1 1 1 1 >

- Amplifiers are finite-gain saturating
- Amplifiers need not be accurate or linear
- Shown for 4-bit
- Same common-mode input on comparators
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators

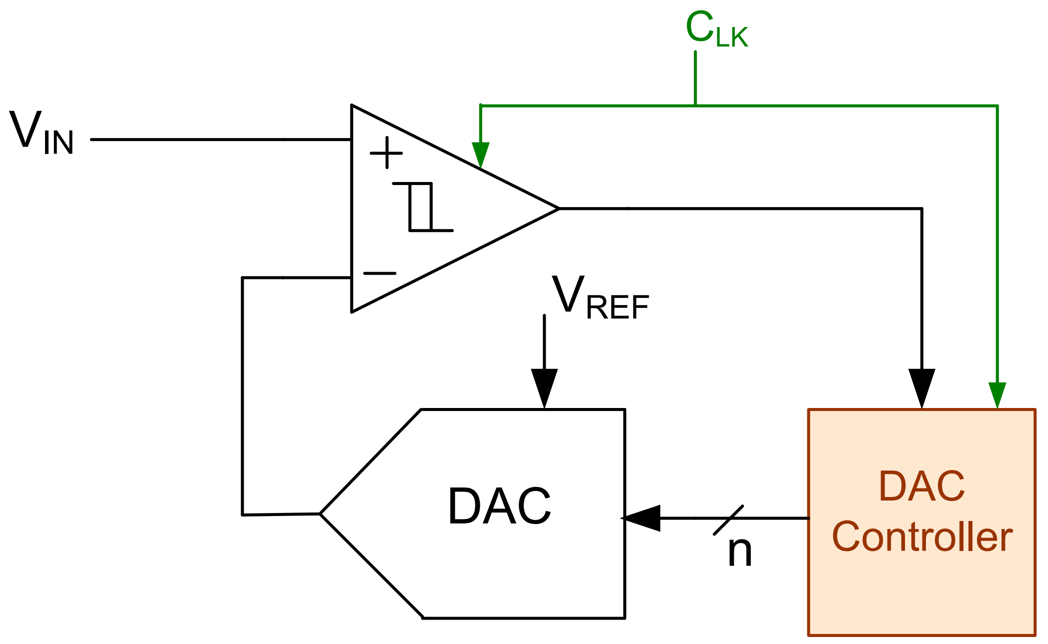


< 1 1 0 0 0 >

Colored bits are shared

Review from Last Lecture

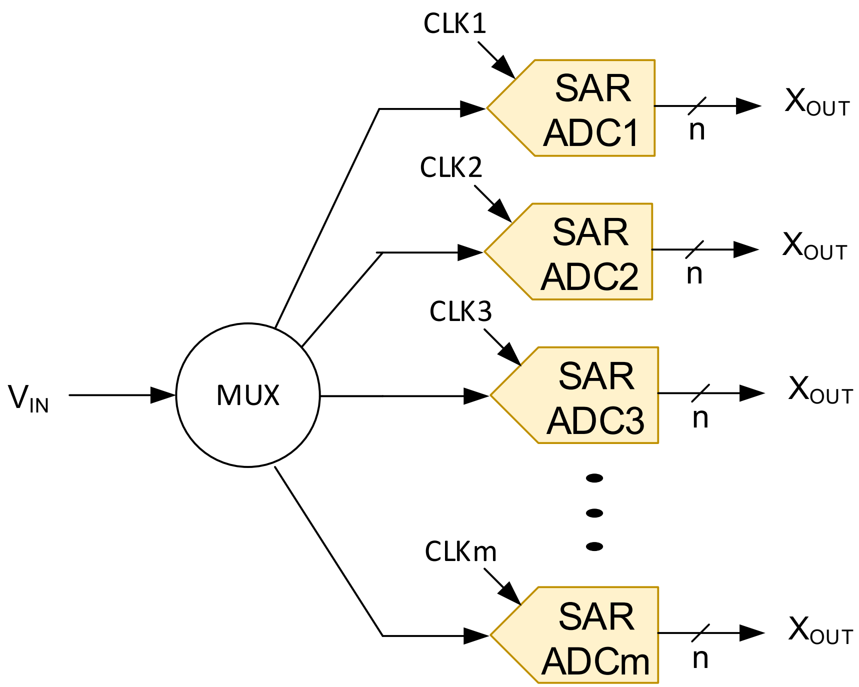
SAR ADC

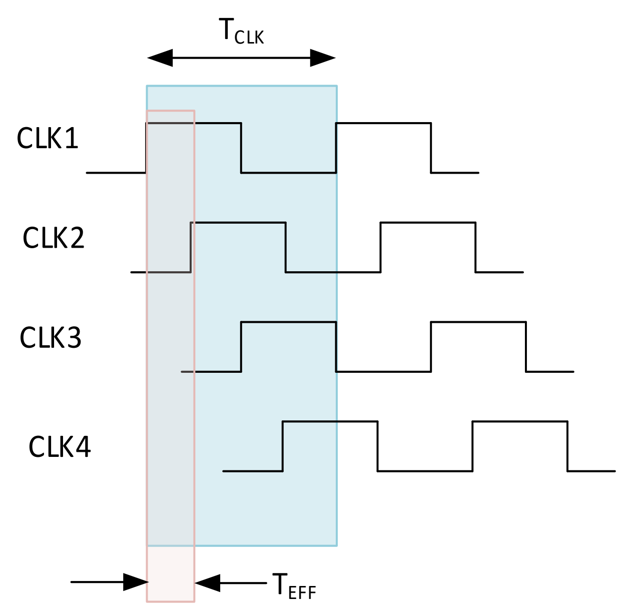


- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small
- Any DAC can be used
- Single comparator !

Review from Last Lecture

Time Interleaved SAR ADC

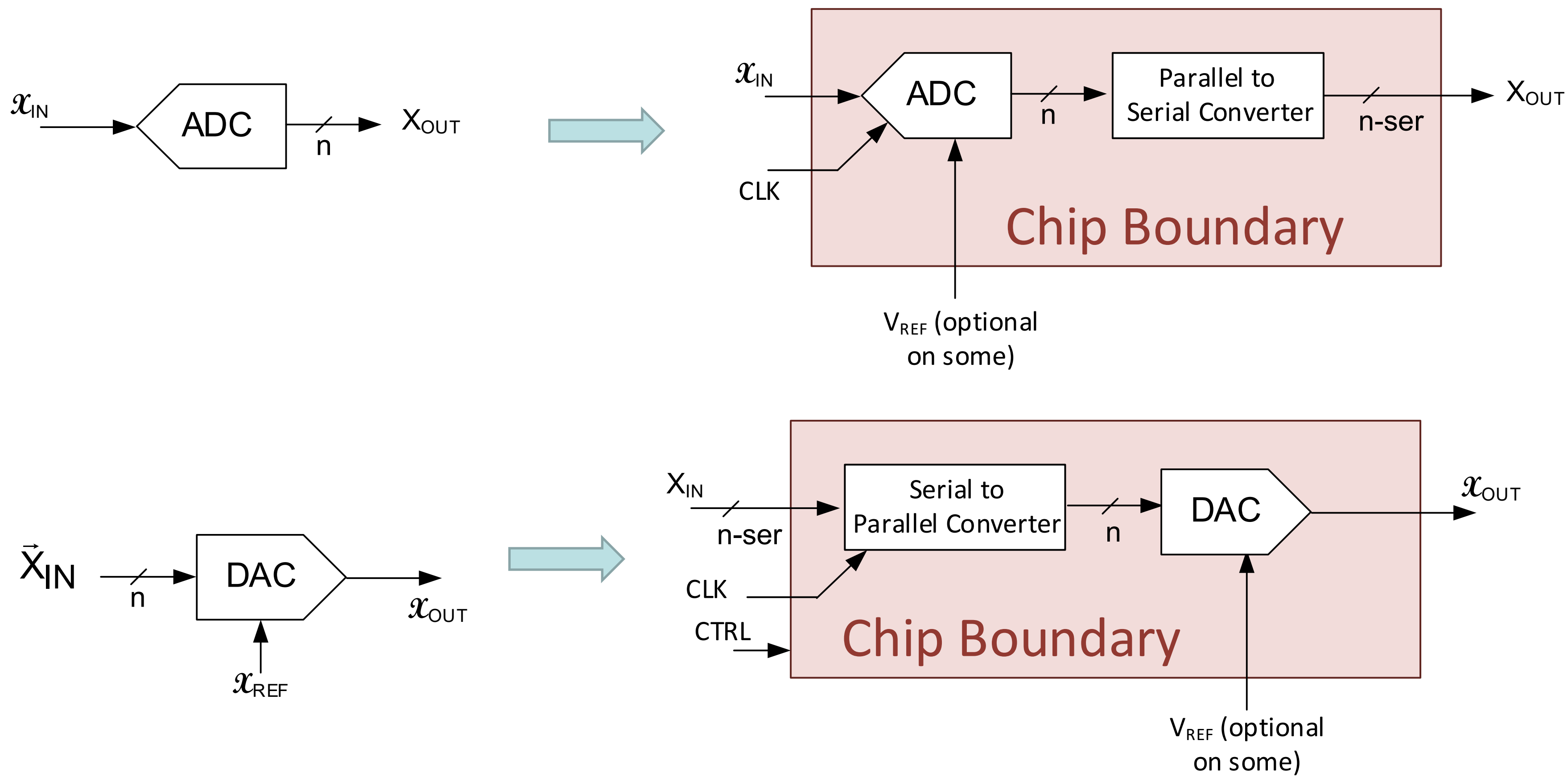




Time interleaving increases effective conversion rate by factor of m

Actual Catalog Data Converter Parts

- Often (not always) digital interface with data converter is serial
- Significantly Reduces pin count
- Interfaces usually follow standard protocols
- Challenge in data converter design almost always in the data converter itself
- Multiple channels often available and these usually use single converter and MUX



Common Application

Want digital representation of analog input at a “distant” location

Distance could be a few cm or thousands of miles

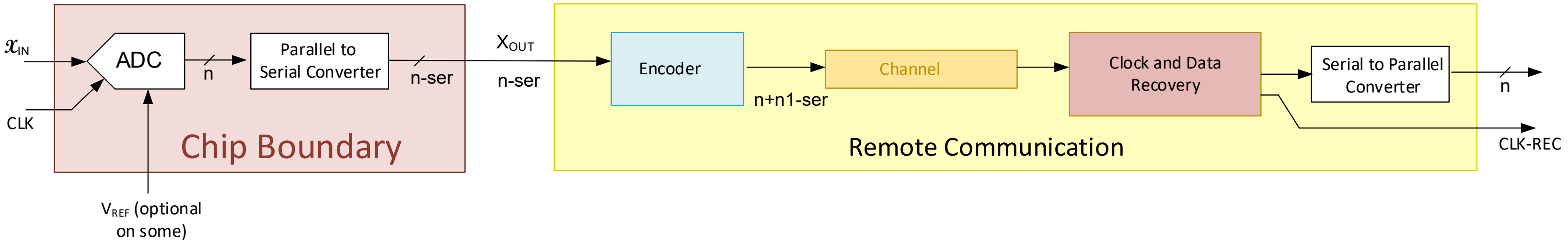
Transmitting clock would dramatically increase communication overhead and provide no additional information

Keeping phase of clock aligned with data would be extremely difficult even for short distances

Data is usually encoded and at receiver end both clock and data are recovered (CDR)

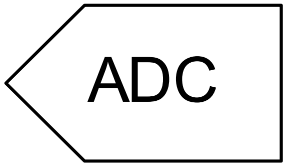
Digital signals themselves degrade when passing through channel

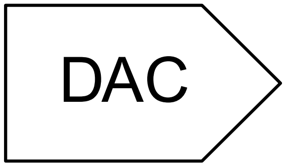
Bit overhead is significant

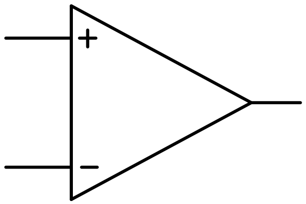


Typical Serial Communication Application of Data Converter

Noise in ADCs and DACs





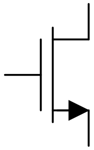


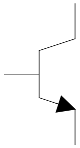
Noise in electronic devices and components introduce noise in electronic systems

Noise is of major concern in ADCs, DADs, and Op Amps

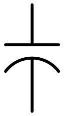
Beyond the scope of this course to go into lots of details about effects of device noise in these components but will provide a brief introduction

Devices that contribute noise :





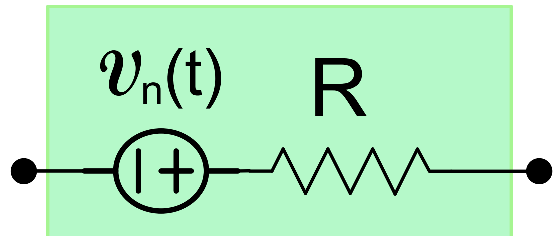
Capacitors and Inductors are noiseless:



Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in resistors:



Noise can be characterized by either $v_n(t)$ (time domain)
or the spectral density S (frequency domain)

Noise spectral density of $v_n(t)$ at all frequencies for a resistor

$$S = 4kTR$$

k: Boltzmann's Constant
T: Temperature in Kelvin

k=1.38064852 × 10^{-23} m^2 kg s^{-2} K^{-1}

At 300K, kT=4.14 x10^{-21}

This is termed white noise because S is independent of f !

Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in linear circuits:

$$v_n(t) \quad \Longleftrightarrow \quad S(f)$$

Typically interested in RMS value of the noise voltage v_{RMS}

Time domain:

$$v_{RMS} = \sqrt{\lim_{T \to \infty} \frac{1}{T} \int_{t=0}^{T} v_n^2(t)\,dt}$$

Difficult to obtain directly !

Frequency domain:

$$\tilde{v}_{RMS} = \sqrt{\int_{f=0}^{\infty} S(f)\,df}$$

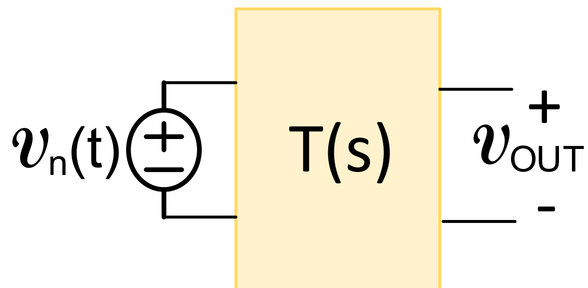
It can be shown that:

$$\tilde{v}_{RMS} = v_{RMS}$$

Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in linear circuits:



Due to any noise voltage source:

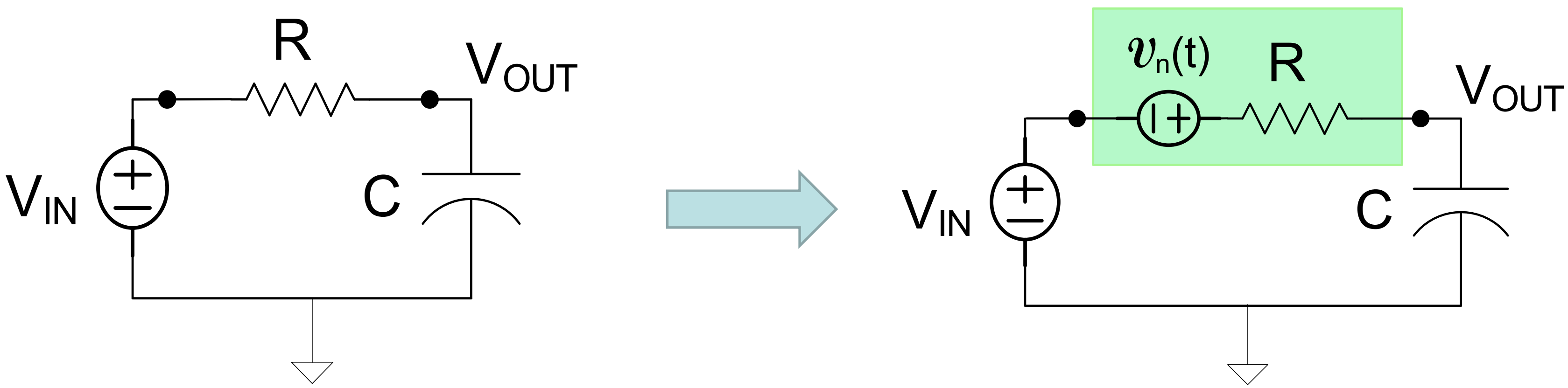
$$S_{V_{OUT}} = S_{V_n} \left| T_n(j\omega) \right|^2$$

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df}$$

Thus:

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \sqrt{\int_{f=0}^{\infty} S_{V_n} \left| T_n(j\omega) \right|^2 df}$$

Example: First-Order RC Network

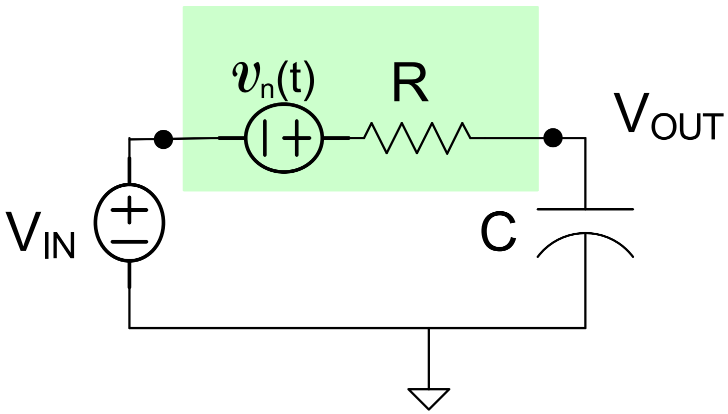


Noise transfer function:
$$T_n(s) = \frac{1}{1+RCs}$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,df}$$

Example: First-Order RC Network

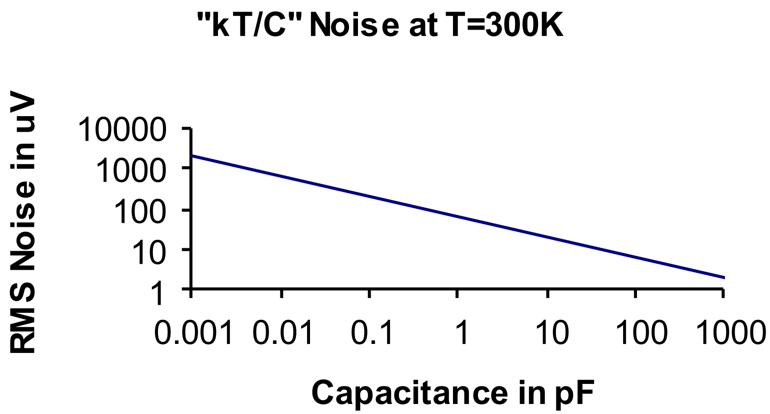


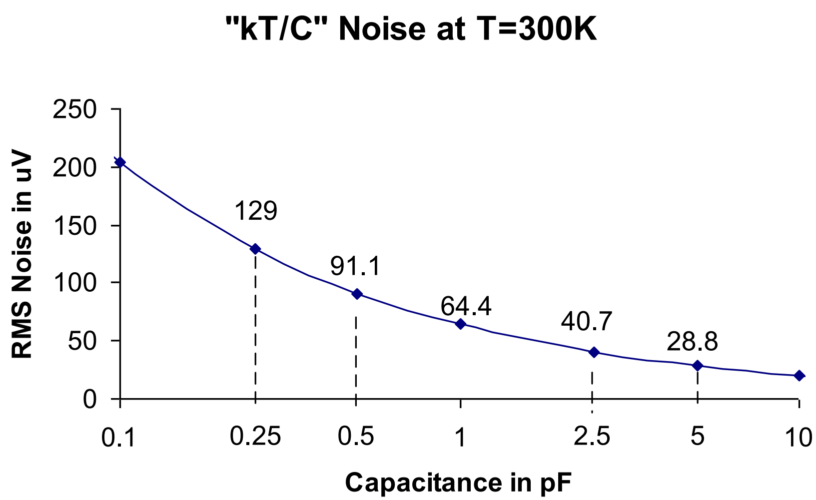
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2 R^2 C^2}\, df}$$

From a standard change of variable with a trig identity, it follows that

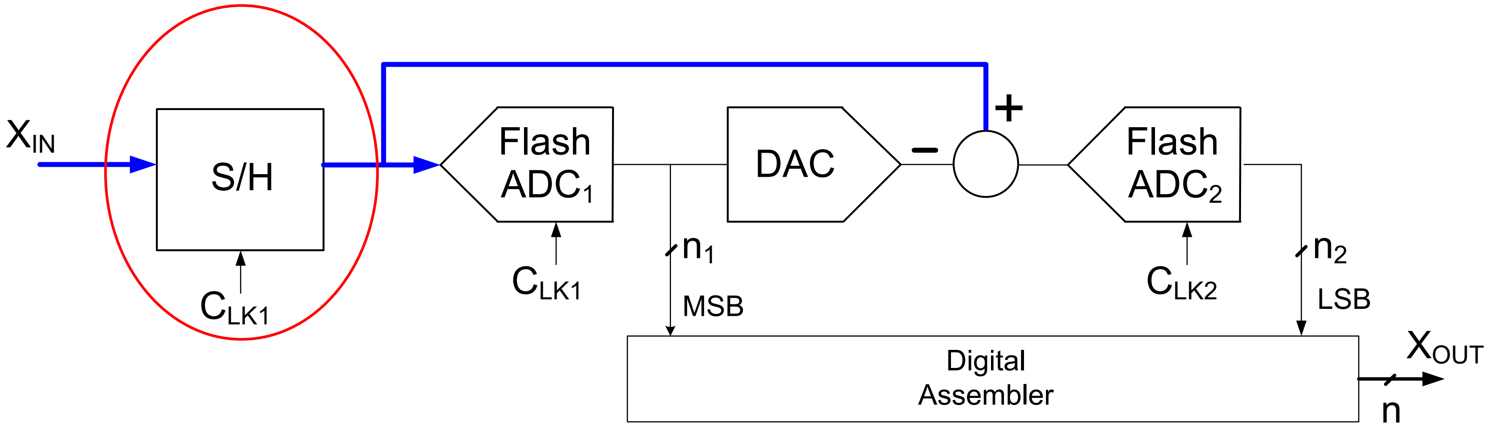
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$

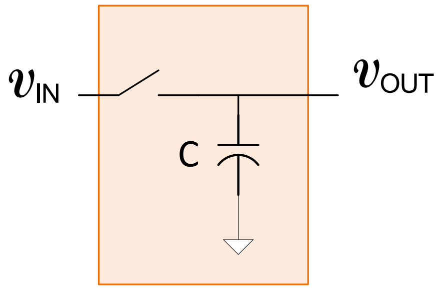
- The continuous-time noise voltage has an RMS value that is independent of R
- Noise contributed by the resistor is dependent only upon the capacitor value C
- This is often referred to at kT/C noise and it can be decreased at a given T only by increasing C

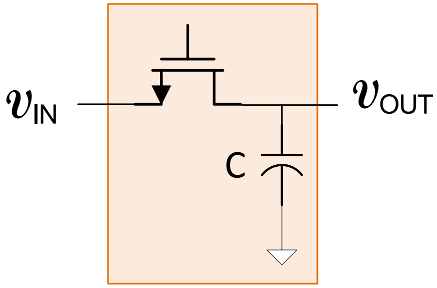

"kT/C" Noise at T=300K
RMS Noise in uV
10000
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Capacitance in pF


"kT/C" Noise at T=300K
RMS Noise in uV
250
200
150
100
50
0
129
91.1
64.4
40.7
28.8
0.1
0.25
0.5
1
2.5
5
10
Capacitance in pF

Sample and Hold Circuits







Basic S/H circuit

Slightly more complicated S/H used for input S/H

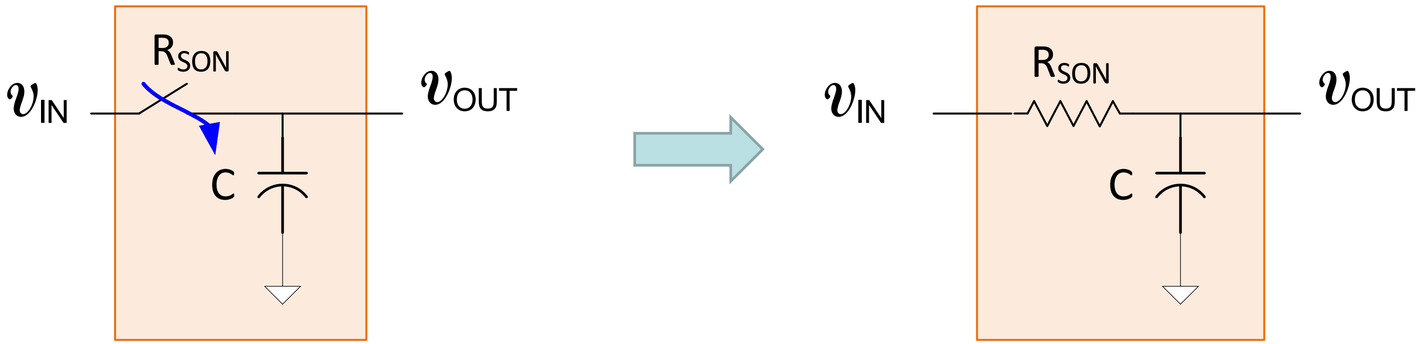
This simple structure used in some applications

Actually a Track and Hold Circuit

Noise characteristics of S/H similar to that of these simple samplers

Sample and Hold Circuits

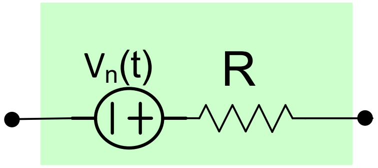
During Track Mode



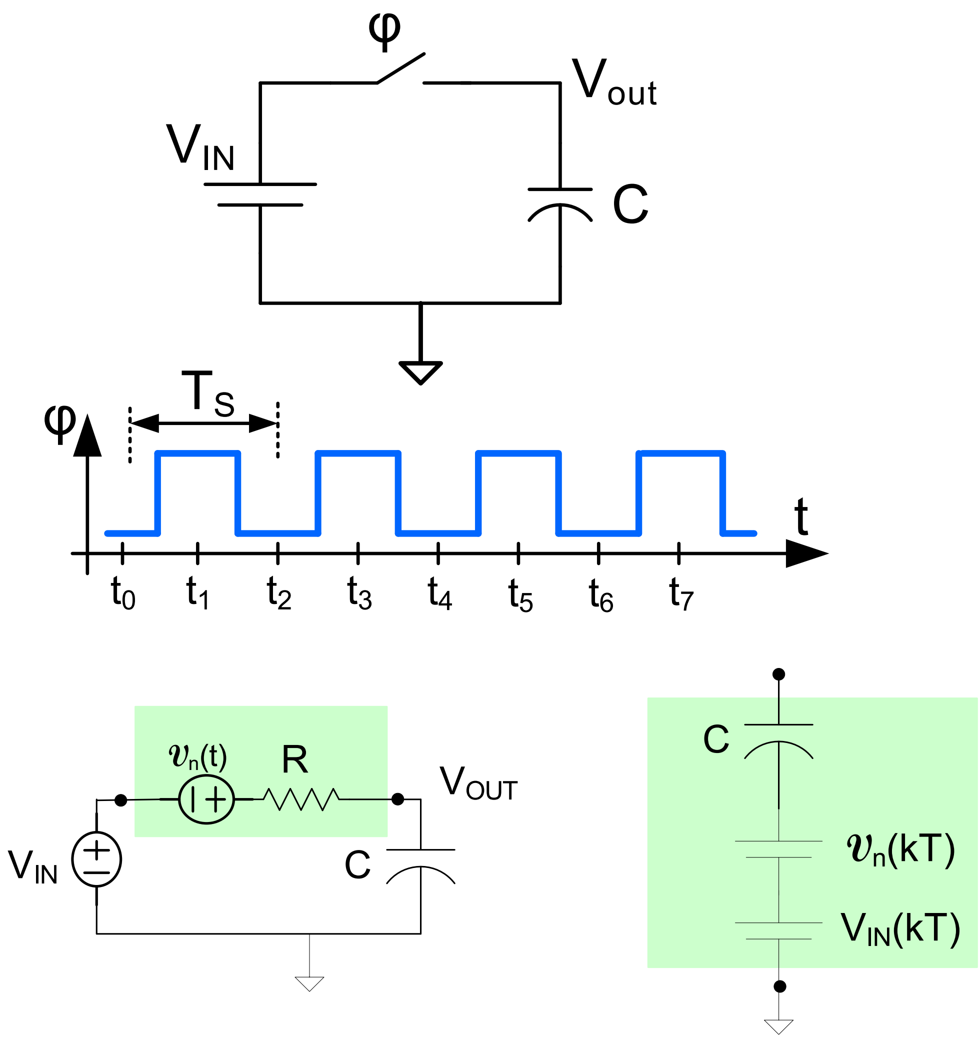
When switch is opened to take sample, noise on C is captured on C (superimposed on signal)

This noise becomes input noise to the ADC

Recall noise in resistor modeled as noise voltage source in series with R



Sample and Hold Circuits



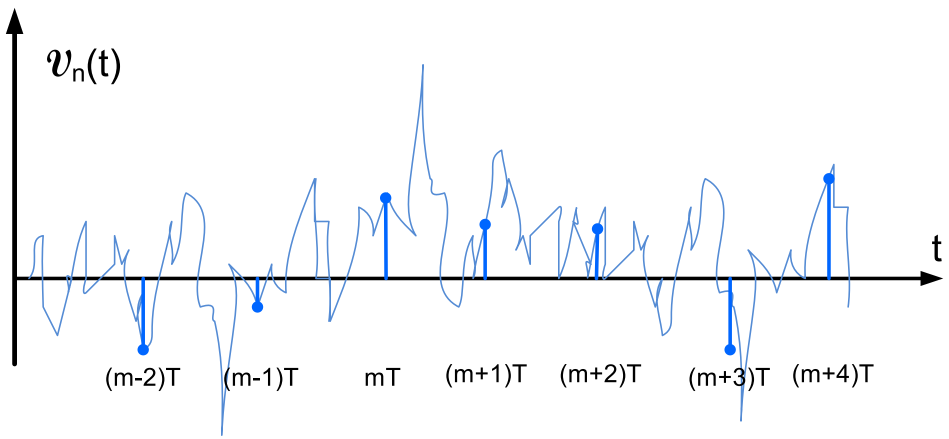
Track mode

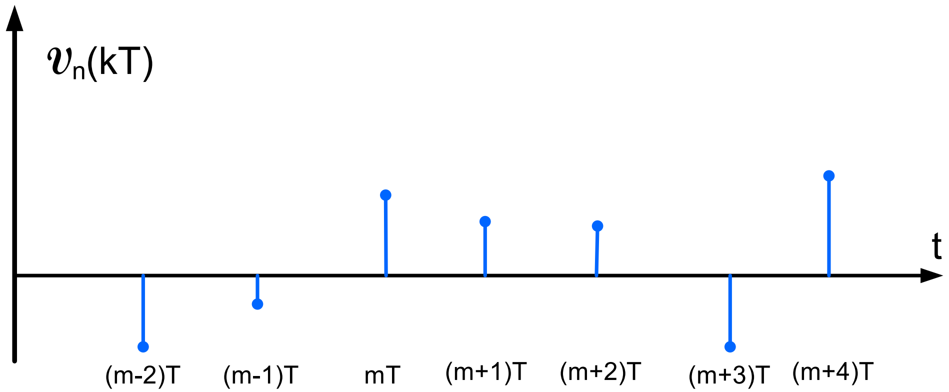
Hold mode

If switch opens fast, noise on C due to R is captured as $v_n(kT)$

Sample and Hold Circuits

T is the period of the sampler

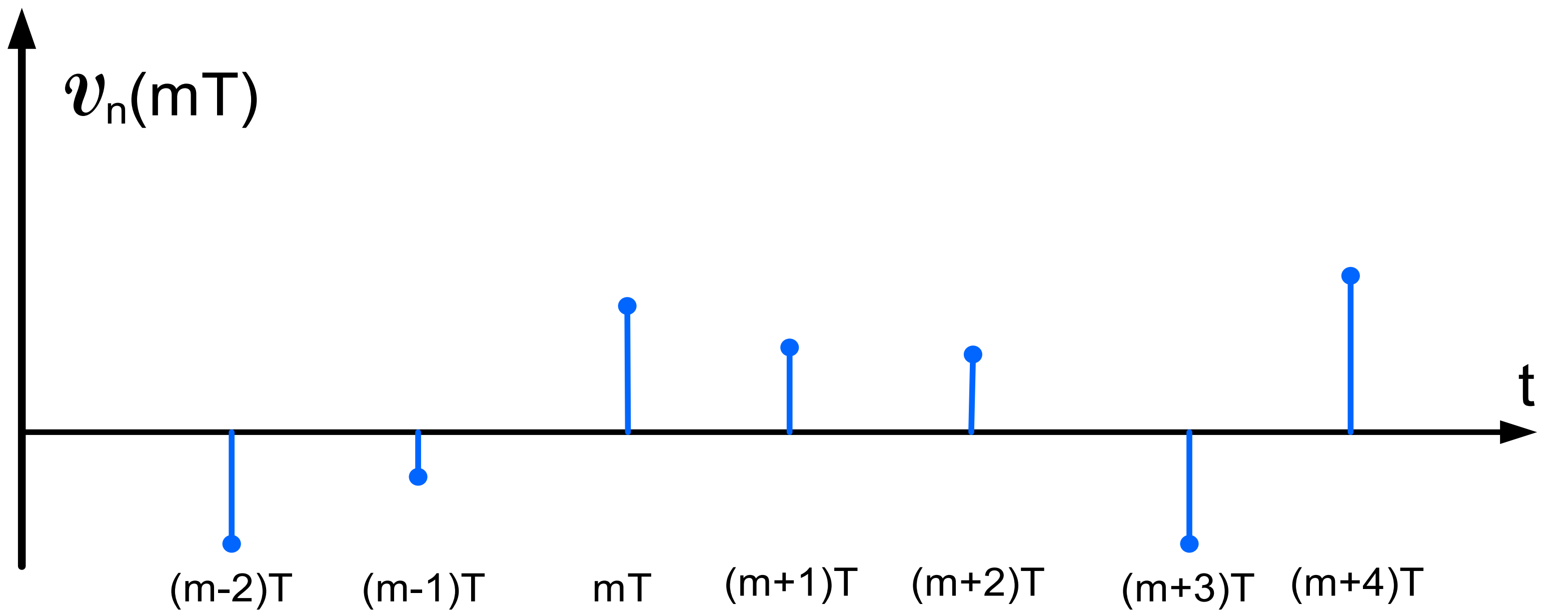




$v_n(mT)$ is a discrete-time sequence obtained by sampling continuous-time noise waveform

RMS value of noise input to pipelined ADC is that of the discrete time noise sequence

Sample and Hold Circuits



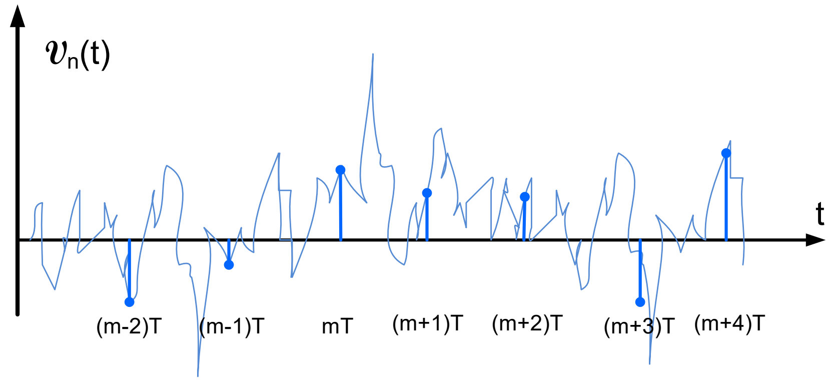
Define the RMS noise of a discrete time noise sequence as

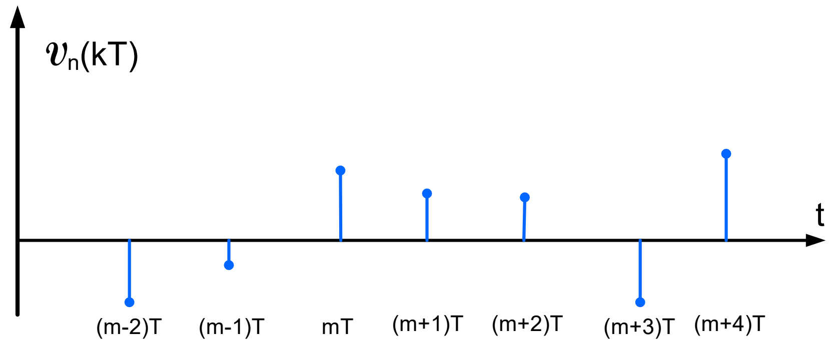
$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right)$$

Thus:

$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right) \underset{N\,large}{\simeq} \sqrt{\frac{1}{N}\sum_{m=1}^{N} v^2(mT)}$$

Sample and Hold Circuits





$v_n(mT)$ for each m is a random variable with some distribution function

This distribution function is independent of m (i.e. the variables are identically distributed)

Assume μ_n is the mean and σ_n is the standard deviation of this random variable

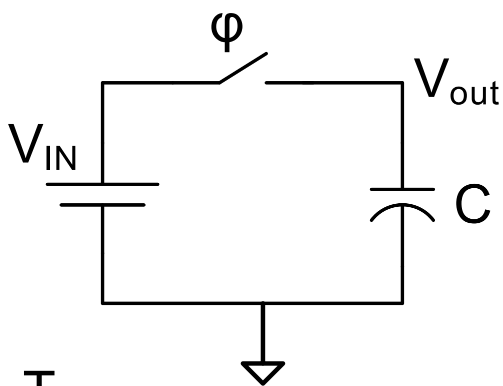
What is the relationship, if any, between $v_{n_{RMS}}$ and $\hat{V}_{RMS}$

Theorem 1 If $\mathcal{V}(t)$ is a continuous-time zero-mean noise source and $<\mathcal{V}(kT)>$ is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as $\mathcal{V}_{RMS} = \hat{\mathcal{V}}_{RMS}$

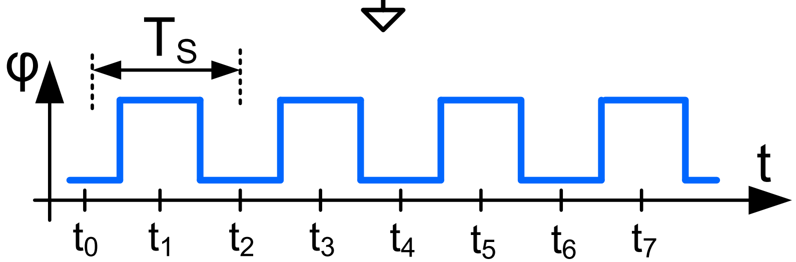
Theorem 2 If $\mathcal{V}(t)$ is a continuous-time zero-mean noise signal and $<\mathcal{V}(kT)>$ is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the standard deviation of the random variable $\mathcal{V}(kT)$, denoted as $\sigma_{\hat{V}}$ satisfies the expression $\sigma_{\hat{V}} = \mathcal{V}_{RMS} = \hat{\mathcal{V}}_{RMS}$

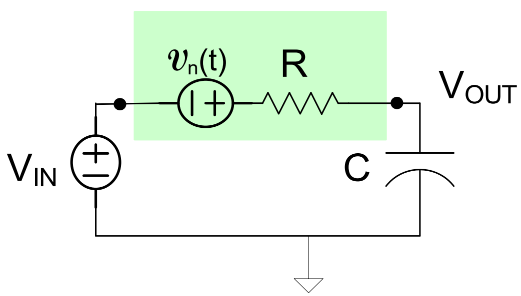
From Theorem 1 we obtain the RMS value of the switched capacitor sampler

Sample and Hold Circuits

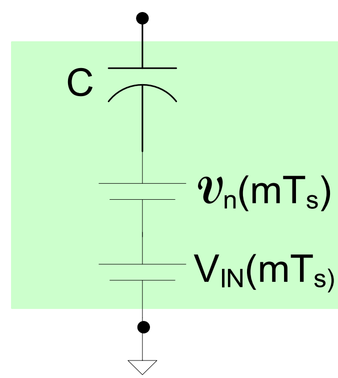


$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$





Track mode



Hold mode

$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

k: Boltzmann’s constant
T: temperature in Kelvin

RMS noise at output of basic SC S/H is independent of R but dependent upon C

Statistical Analysis of Data Converters

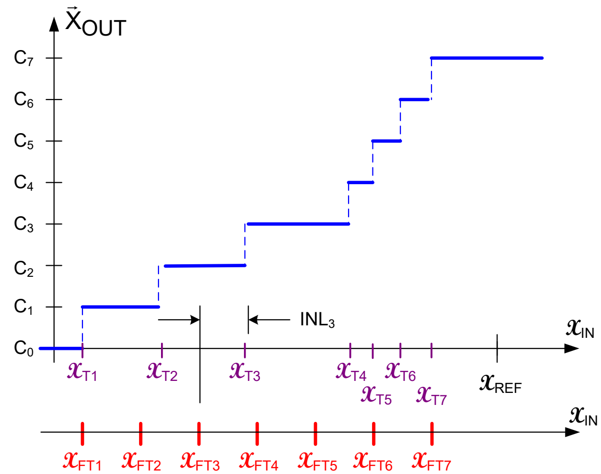
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$\mathrm{INL_k} = \frac{x_{\mathrm{Tk}} - x_{\mathrm{FTk}}}{x_{\mathrm{LSB}}} \qquad 1 \le \mathrm{k} \le \mathrm{N\text{-}2}$$

$$\mathrm{INL} = \max_{2 \le \mathrm{k} \le \mathrm{N\text{-}2}} \left\{ \left| \mathrm{INL_k} \right| \right\}$$



- Component dimensions and model parameters of all devices in a data converter are actually random variables at the design stage!
- At design stage, INL characterized by standard deviation of many random variables
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - -Model parameters become random variables
  - -Process parameters affect multiple model parameters causing model parameter correlation
  - -Simulation times can become very large

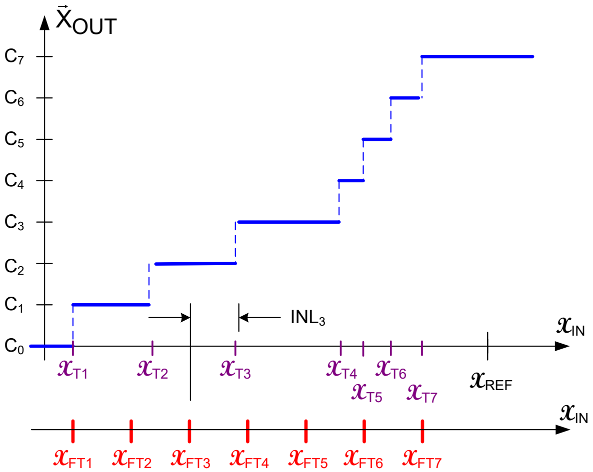
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$\mathrm{INL}_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$\mathrm{INL} = \max_{2 \le k \le N-2} \left\{ \left| \mathrm{INL}_k \right| \right\}$$



- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- Expected value of INL_k at k=(N-1)/2 is largest for many architectures
- INL of $\frac{x_{LSB}}{2}$ often considered acceptable (this is the ideal value of the continuous-input INL

  definition though many high-speed ADCs and some lower-speed structures will have an INL that exceeds this)

- Major effort in ADC design is in obtaining an INL acceptable yield !
- Yield often strongly dependent upon matching of random variables !

Characteristics of Data Converters Dominantly Depend Upon Random Variables

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Characteristics of Data Converters Dominantly Depend Upon Random Variables

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

Methods of Characterizing how Random Variables Affect Performance

- Analytical Statistical Formulation and Analysis
- MATLAB Simulations (often using Monte-Carlo Analysis)
- Spectre/Spice Monte-Carlo Simulations
- Ignore Effects of Random Effects

How important is statistical characterization of data converters?

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC

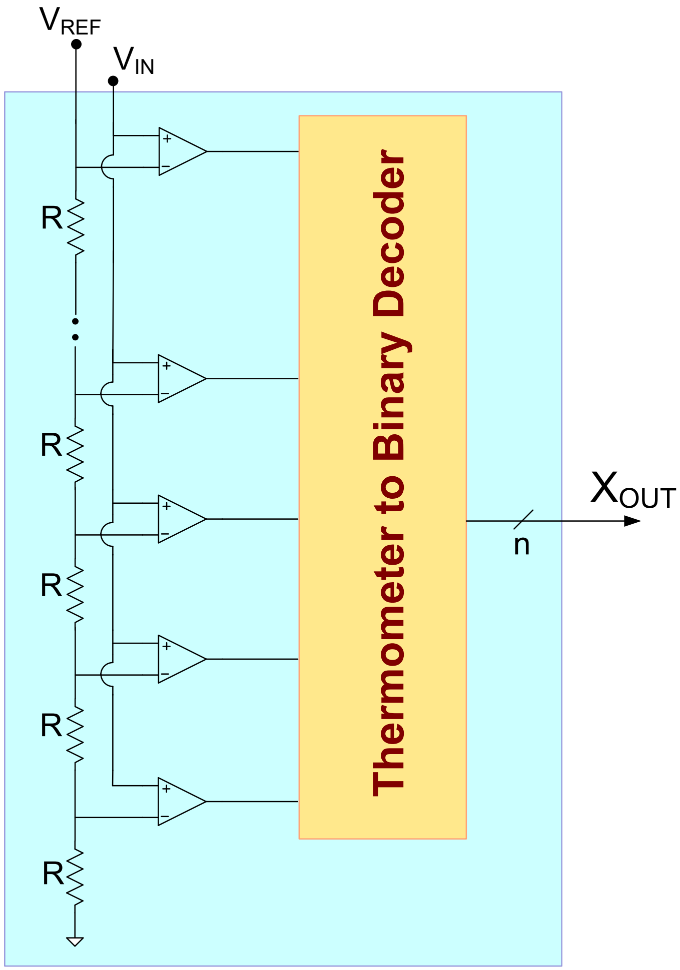
Assume R-string is ideal, V_{REF}=1V and V_{OS} for each comparator must be at most +/- ½ LSB

Why this assumption?

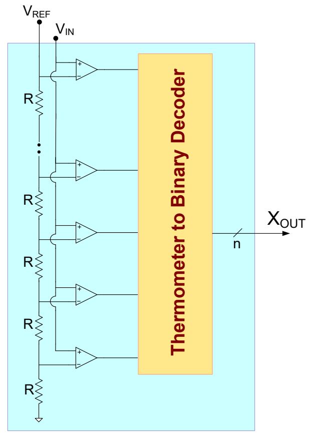
Note: this is a much different performance requirement than requiring that INL< ½ LSB and would not be part of a standard specification but we will see that it is analytical tractable and gives an appreciation for the importance of statistical analysis

Case 1

Determine the yield if V_{OS} has a Gaussian distribution (Normal) with zero mean and a standard deviation of 5mV



How important is statistical analysis?



Example: 7-bit FLASH ADC with R-string DAC

Assume R-string is ideal, V_{REF}=1V and V_{OS} for each comparator must be at most +/- ½ LSB

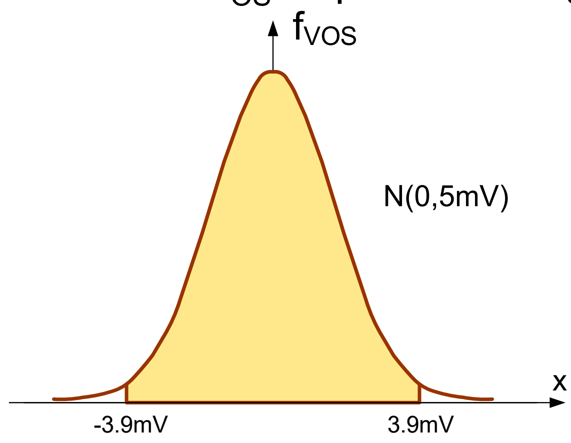
Case 1

Determine the yield if V_{OS} has a Gaussian distribution (Normal) with zero mean and a standard deviation of 5mV

$$\tfrac{1}{2}\text{ LSB} = 1V/(2^{(7+1)})=3.9mV$$

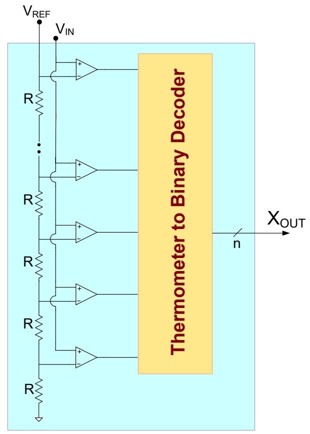
The probability that a single comparator meets the V_{OS} requirement is given by

$$P_{COMP} = \int_{-3.9mV}^{3.9mV} f_{VOS}\,dV$$



How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC
Assume V_{OS} is zero-mean gaussian



Case 1 σ_{VOS}=5mV

$$P_{COMP} = \int_{-3.9mV}^{3.9mV} f_{VOS} dV$$

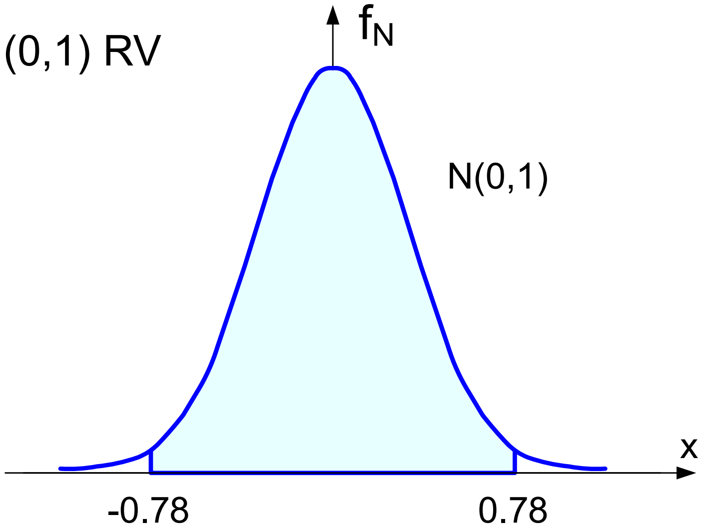
Define $X_N = V_{OS}/\sigma$ Since μ=0, this will make X_N : N(0,1)

$$P_{COMP} = \int_{-X_N}^{X_N} f_N dx$$

f_N and F_N are pdf and cdr of N(0,1) RV

X_N=3.9mV/5mV=0.78

$$P_{COMP} = \int_{-0.78}^{0.78} f_N dx$$



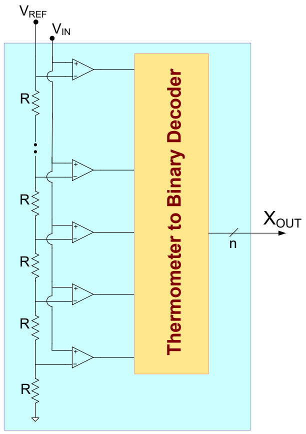
$$P_{COMP} = 2 \bullet F_N(0.78) - 1$$

Table of CDF for N(0,1) Random Variables

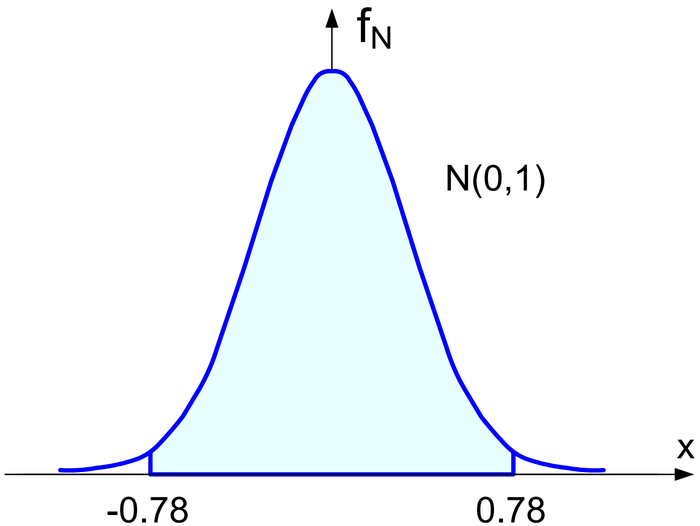
z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
0.2	0.5793	0.5832	0.5871	0.5910	0.5948	0.5987	0.6026	0.6064	0.6103	0.6141
0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
0.5	0.6915	0.6950	0.6985	0.7019	0.7054	0.7088	0.7123	0.7157	0.7190	0.7224
0.6	0.7257	0.7291	0.7324	0.7357	0.7389	0.7422	0.7454	0.7486	0.7517	0.7549
0.7	0.7580	0.7611	0.7642	0.7673	0.7703	0.7734	0.7764	0.7794	0.7823	0.7852
0.8	0.7881	0.7910	0.7939	0.7967	0.7995	0.8023	0.8051	0.8078	0.8106	0.8133
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.90147
1.3	0.90320	0.90490	0.90658	0.90824	0.90988	0.91149	0.91309	0.91466	0.91621	0.91774
1.4	0.91924	0.92073	0.92220	0.92364	0.92507	0.92647	0.92785	0.92922	0.93056	0.93189
1.5	0.93319	0.93448	0.93574	0.93699	0.93822	0.93943	0.94062	0.94179	0.94295	0.94408
1.6	0.94520	0.94630	0.94738	0.94845	0.94950	0.95053	0.95154	0.95254	0.95352	0.95449
1.7	0.95543	0.95637	0.95728	0.95818	0.95907	0.95994	0.96080	0.96164	0.96246	0.96327
1.8	0.96407	0.96485	0.96562	0.96638	0.96712	0.96784	0.96856	0.96926	0.96995	0.97062
1.9	0.97128	0.97193	0.97257	0.97320	0.97381	0.97441	0.97500	0.97558	0.97615	0.97670
2.0	0.97725	0.97778	0.97831	0.97882	0.97932	0.97982	0.98030	0.98077	0.98124	0.98169
2.1	0.98214	0.98257	0.98300	0.98341	0.98382	0.98422	0.98461	0.98500	0.98537	0.98574
2.2	0.98610	0.98645	0.98679	0.98713	0.98745	0.98778	0.98809	0.98840	0.98870	0.98899
2.3	0.98928	0.98956	0.98983	$0.9^{2}0097$	$0.9^{2}0358$	$0.9^{2}0613$	$0.9^{2}0863$	$0.9^{2}1106$	$0.9^{2}1344$	$0.9^{2}1576$
2.4	$0.9^{2}1802$	$0.9^{2}2024$	$0.9^{2}2240$	$0.9^{2}2451$	$0.9^{2}2656$	$0.9^{2}2857$	$0.9^{2}3053$	$0.9^{2}3244$	$0.9^{2}3431$	$0.9^{2}3613$
2.5	$0.9^{2}3790$	$0.9^{2}3963$	$0.9^{2}4132$	$0.9^{2}4297$	$0.9^{2}4457$	$0.9^{2}4614$	$0.9^{2}4766$	$0.9^{2}4915$	$0.9^{2}5060$	$0.9^{2}5201$
2.6	$0.9^{2}5339$	$0.9^{2}5473$	$0.9^{2}5604$	$0.9^{2}5731$	$0.9^{2}5855$	$0.9^{2}5975$	$0.9^{2}6093$	$0.9^{2}6207$	$0.9^{2}6319$	$0.9^{2}6427$
2.7	$0.9^{2}6533$	$0.9^{2}6636$	$0.9^{2}6736$	$0.9^{2}6833$	$0.9^{2}6928$	$0.9^{2}7020$	$0.9^{2}7110$	$0.9^{2}7197$	$0.9^{2}7282$	$0.9^{2}7365$
2.8	$0.9^{2}7445$	$0.9^{2}7523$	$0.9^{2}7599$	$0.9^{2}7673$	$0.9^{2}7744$	$0.9^{2}7814$	$0.9^{2}7882$	$0.9^{2}7948$	$0.9^{2}8012$	$0.9^{2}8074$
2.9	$0.9^{2}8134$	$0.9^{2}8193$	$0.9^{2}8250$	$0.9^{2}8305$	$0.9^{2}8359$	$0.9^{2}8411$	$0.9^{2}8462$	$0.9^{2}8511$	$0.9^{2}8559$	$0.9^{2}8605$
3.0	$0.9^{2}8650$	$0.9^{2}8694$	$0.9^{2}8736$	$0.9^{2}8777$	$0.9^{2}8817$	$0.9^{2}8856$	$0.9^{2}8893$	$0.9^{2}8930$	$0.9^{2}8965$	$0.9^{2}8999$

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC

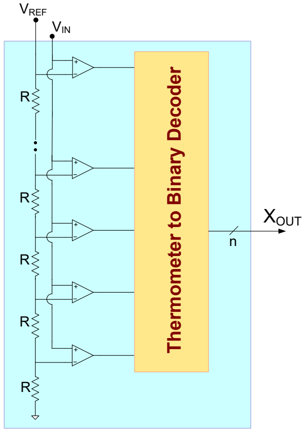


$$P_{COMP} = 2 \bullet F_N(0.78) - 1 = 2 \bullet .7823 - 1 = 0.565$$



Each comparator has 56.5% yield

How important is statistical analysis?



Example: 7-bit FLASH ADC with R-string DAC

Case 1 σ_{VOS}=5mV

$P_{COMP} = 0.565$

Since all comparators must be good, the ADC yield is

$$Y_{ADC}=(P_{COMP})^{127}=(0.565)^{127}$$

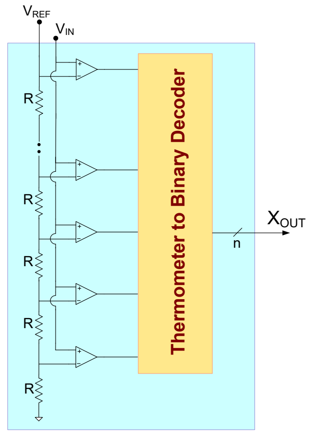
$$Y_{ADC}=3.2\bullet 10^{-32}$$

This yield is essentially 0 and a standard deviation of 5mV is even not trivial to obtain with MOS comparators !

The effects of statistical variation can have dramatic effects on yield of data converters !

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC



Case 1 σ_{VOS}=5mV

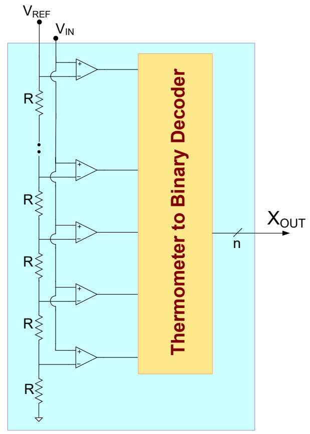
Since all comparators must be good, the ADC yield is

$$Y_{ADC}=3.2\bullet 10^{-32}$$

Note: The specification in this example that requires no comparator has an offset voltage of larger than 0.5LSB may not be a good performance specification as the FLASH ADC may actually perform reasonably well even if some comparators have an offset that is larger than 0.5LSB. A more useful requirement might be that there be no bubbles in the thermometer code output. Certainly if all comparators have an offset that is at most 0.5LSB, there will be no bubbles in the output code attributable to comparator offset but a modestly weaker constraint can also guarantee there are no bubbles. With the 0.5LSB assumption, a specification that was dependent upon 127 uncorrelated random variables was obtained which made the analysis quite easy. A “no bubble” specification could be approximated by stating that the maximum of the 127 V_{OSk}-V_{OSk-1}must be less than V_{LSB}. This becomes an order statistic of 127 Gaussian random variables which is analytically intractable.

How important is statistical analysis?

Example: 7-bit FLASH ADC with R-string DAC



Case 2 Repeat the previous example if σ_{VOS}=1mV

Assume R-string is ideal, V_{REF}=1V and V_{OS} for each comparator must be at most +/- ½ LSB

$$P_{COMP} = \int_{-3.9mV}^{3.9mV} f_{VOS} dV$$

X_N=3.9mV/1mV=3.9

$$P_{COMP} = \int_{-3.9}^{3.9} f_N dx \qquad P_{COMP} = 2 \bullet F_N(3.9) - 1 = 2 \bullet 0.999952 - 1 = 0.999904$$

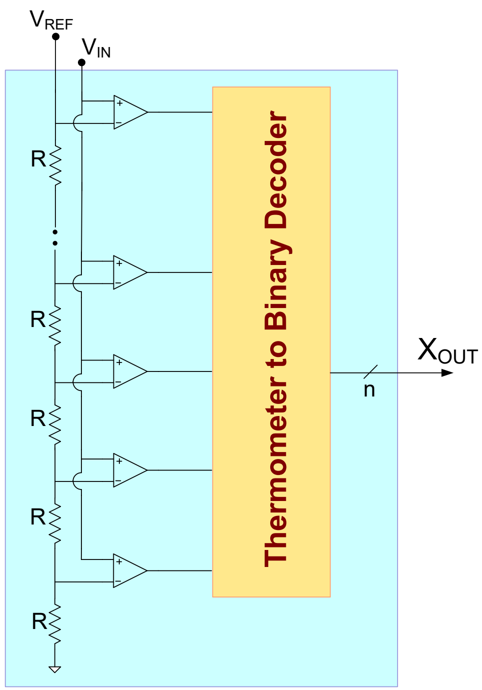
$$Y_{ADC} = (P_{COMP})^{127} = (0.999904)^{127}$$

$$Y_{ADC} = 0.988$$

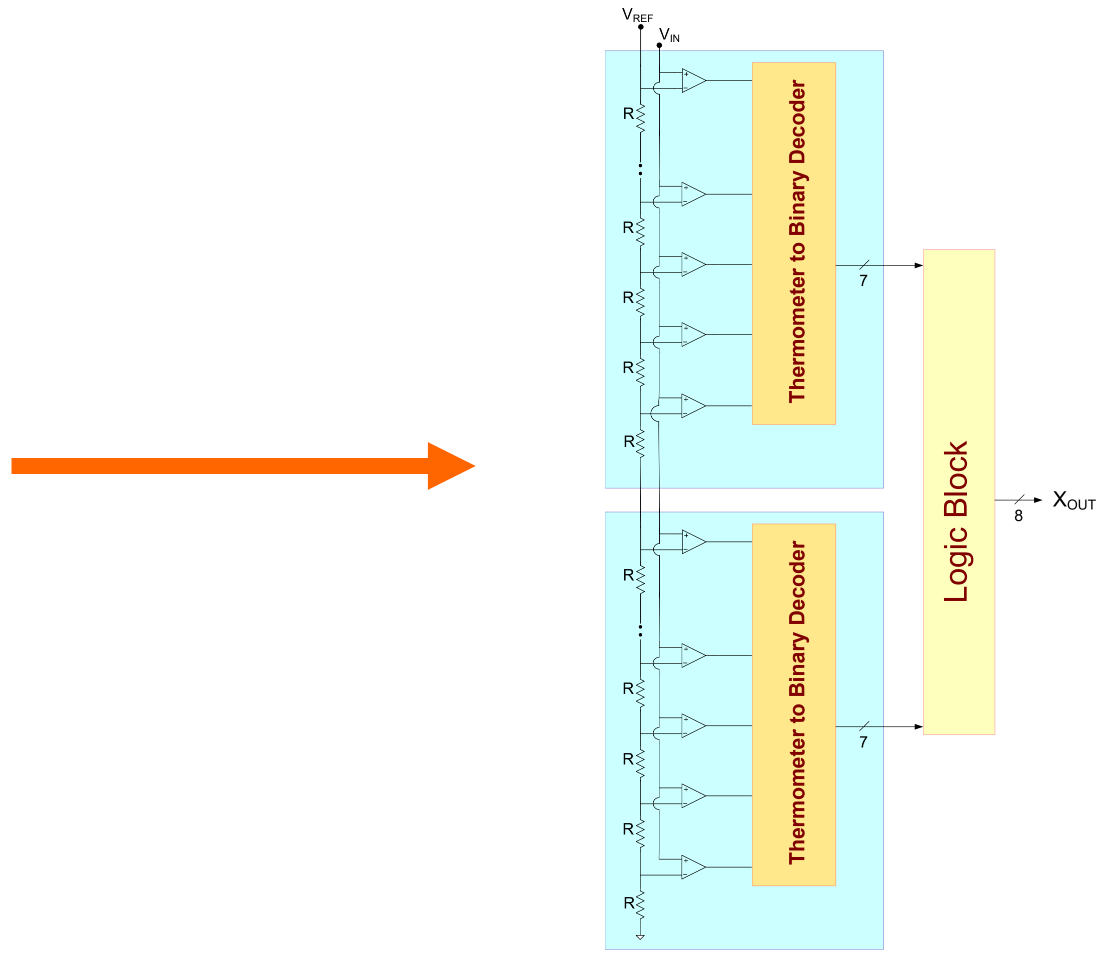
This modest change in the offset voltage has increased the yield to 98.8%

How important is statistical analysis?

Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?



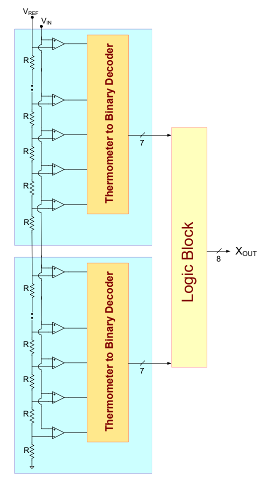
Y_{ADC}=98.8%



Y_{ADC}=?

How important is statistical analysis?

Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?



Since one additional bit has been added, V_{LSB} will decrease From 7.8mV to 3.9mV. Thus ½ LSB will be reduced to 1.95mV

$$P_{COMP} = \int_{-1.95mV}^{1.95mV} f_{VOS} dV$$

With the same σ_{VOS}=1mV, X_N=1.95mV/1mV=1.95

$$P_{COMP} = \int_{-1.95}^{1.95} f_N dx \qquad P_{COMP} = 2 \bullet F_N(1.95) - 1 = 2 \bullet 0.97441 - 1 = 0.9488$$

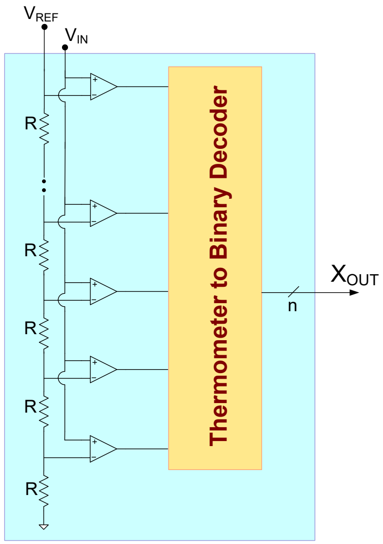
$$Y_{ADC} = (P_{COMP})^{255} = (0.9488)^{255}$$

$$Y_{ADC} = 1.52 \bullet 10^{-6}$$

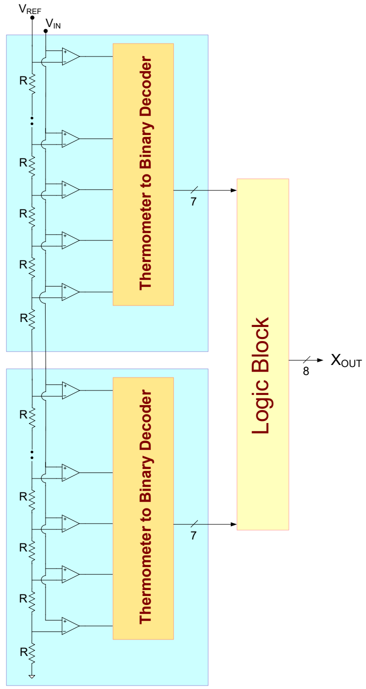
This seemingly simple extension of a circuit with a very high yield has essentially no yield !

How important is statistical analysis?

Example: What will be the yield if two of the 7-bit FLASH ADCs with yields of 98.8% are combined to obtain an 8-bit ADC?



Y_{ADC}=98.8%



$Y_{ADC}=1.52\bullet 10^{-6}$

- The onset of statistically-induced yield loss can be abrupt
- Intuition is not an acceptable substitute to statistical analysis
- Without statistical analysis/simulation there is a high probability that a data converter will be substantially over designed or under designed and neither is acceptable

Statistical Modeling of Random Variations

For the effects of local random variations of a parameter X, generally

$$\sigma_X \propto \frac{A_0}{\sqrt{A_C}}$$

where A_C is the area of the matching critical components and A_0 is a process parameter

Importance of statistical analysis – example

What changes in area would be needed to decrease σ_{VOS} from 5mV to 1mV?

$$\sigma_X \propto \frac{A_0}{\sqrt{A_C}}$$

$$\left.\begin{aligned} \sigma_{X_5} &= \theta \frac{A_0}{\sqrt{A_{C_5}}} \\ \sigma_{X_1} &= \theta \frac{A_0}{\sqrt{A_{C_1}}} \end{aligned}\right\} \Rightarrow \frac{\sigma_{X_5}}{\sigma_{X_1}} = \frac{\sqrt{A_{C_1}}}{\sqrt{A_{C_5}}} = 5$$

$$A_{C_1} = 25 A_{C_5}$$

Equivalent Number of Bits (ENOB)

- Often the performance of an n-bit commercial data converter is not commensurate with that of an ideal n-bit data converter but more like that of an n-k bit data converter
- The equivalent number of bits (ENOB) is often used to characterize the actual level of performance
- Different ENOB definitions depending upon which characterization parameter is of interest

  (e.g. INL, SFDR, SNR, …)

INL-based ENOB

(Review from Lecture 27 Spring 2023)

Consider initially the continuous INL definition for an ADC where the INL of an ideal ADC is $X_{LSB}/2$

Assume $$INL = \upsilon X_{LSBR} = \upsilon \frac{X_{REF}}{2^{n_R}}$$

where X_{LSBR} is the LSB based upon the defined resolution , n_R

Define the equivalent LSB by $$X_{LSBE} = \frac{X_{REF}}{2^{n_{EQ}}}$$

Thus (substituting for X_{REF} into INL expression):

$$INL = \upsilon \frac{2^{n_{EQ}}}{2^{n_R}} X_{LSBE} = \left[\upsilon 2^{n_{EQ}+1-n_R} \right] \frac{X_{LSBE}}{2}$$

Since an ideal ADC has an INL of $X_{LSB}/2$, Setting term in [ ] to 1, can solve for n_{EQ} to obtain

$$ENOB = n_{EQ} = \log_2\left(\frac{1}{2\theta}\right) = n_R - 1 - \log_2(\upsilon)$$

where n_R is the defined resolution

(Review from Lecture 27 Spring 2023)

INL-based ENOB

$$\text{ENOB} = n_R - 1 - \log_2(\upsilon)$$

Consider an ADC with specified resolution of n_R and INL of v LSB

ν	ENOB
½	n_R
1	n_R-1
2	n_R-2
4	n_R-3
8	n_R-4
16	n_R-5

Though based upon the continuous-INL definition, often used to define ENOB from INL viewpoint

ANALOG DEVICES

16-Bit, 200 MSPS/250 MSPS Analog-to-Digital Converter

Data Sheet $120 in 1000's **AD9467**

FEATURES

- 75.5 dBFS SNR to 210 MHz at 250 MSPS
- 90 dBFS SFDR to 300 MHz at 250 MSPS
- SFDR at 170 MHz at 250 MSPS
  - 92 dBFS at −1 dBFS
  - 100 dBFS at −2 dBFS
- 60 fs rms jitter
- Excellent linearity at 250 MSPS
  - DNL = ±0.5 LSB typical
  - INL = ±3.5 LSB typical
- 2 V p-p to 2.5 V p-p (default) differential full-scale input (programmable)
- Integrated input buffer
- External reference support option
- Clock duty cycle stabilizer
- Output clock available
- Serial port control
  - Built-in selectable digital test pattern generation
  - Selectable output data format
- LVDS outputs (ANSI-644 compatible)
- 1.8 V and 3.3 V supply operation

FUNCTIONAL BLOCK DIAGRAM

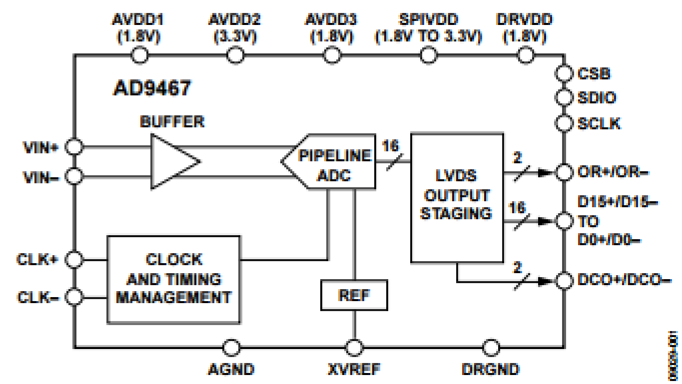


Figure 1.

$$\text{ENOB} = n_R - 1 - \log_2(\upsilon) = 16 - 1 - 1.85 \cong 13.15$$

Is this close to 16-bit performance?

APPLICATIONS

- Multicarrier, multimode cellular receivers
- Antenna array positioning
- Power amplifier linearization
- Broadband wireless
- Radar
- Infrared imaging
- Communications instrumentation

A data clock output (DCO) for capturing data on the output is provided for signaling a new output bit.

The internal power-down feature supported via the SPI typically consumes less than 5 mW when disabled.

Optional features allow users to implement various selectable operating conditions, including input range, data format select, and output data test patterns.

The AD9467 is available in a Pb-free, 72-lead, LFCSP specified over the −40°C to +85°C industrial temperature range.

Can we depend on this “13-bit” INL performance?

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

$$\text{ENOB} = n_R - 1 - \log_2(\upsilon) = 16 - 1 - 3.58 \cong 11.42$$

From INL viewpoint, performance of marketed parts could be about 4.5 bits less than physical resolution but does have other attractive properties

AC SPECIFICATIONS

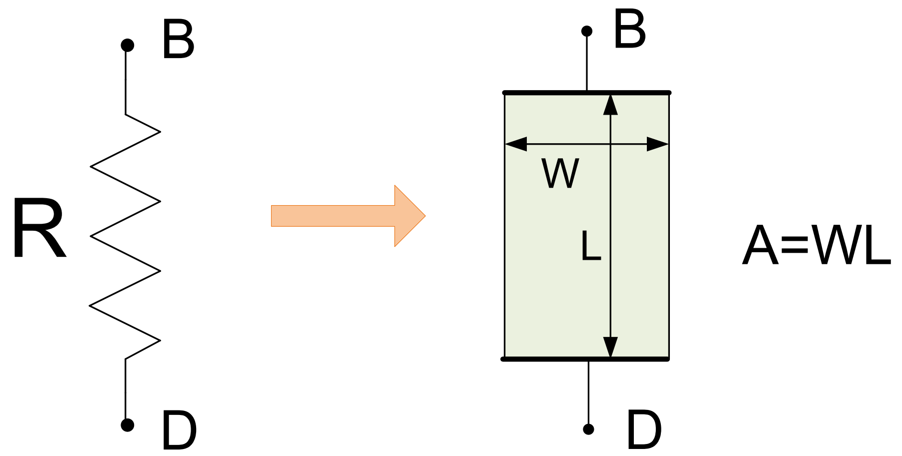
AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
ANALOG INPUT FULL SCALE		2.5	2/2.5		V p-p
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 5 MHz	25°C		74.7/76.4		dBFS
f_{IN} = 97 MHz	25°C		74.5/76.1		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	73.7	74.3/75.8		dBFS
	Full	71.5			dBFS
f_{IN} = 210 MHz	25°C		74.0/75.5		dBFS
f_{IN} = 300 MHz	25°C		73.3/74.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)					
f_{IN} = 5 MHz	25°C		74.6/76.3		dBFS
f_{IN} = 97 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 140 MHz	25°C		74.4/76.0		dBFS
f_{IN} = 170 MHz	25°C	72.4	74.2/75.8		dBFS
	Full	71.0			dBFS
f_{IN} = 210 MHz	25°C		73.9/75.4		dBFS
f_{IN} = 300 MHz	25°C		73.1/74.4		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 5 MHz	25°C		12.1/12.4		Bits
f_{IN} = 97 MHz	25°C		12.1/12.3		Bits
f_{IN} = 140 MHz	25°C		12.1/12.3		Bits
f_{IN} = 170 MHz	25°C		12.0/12.3		Bits
	Full	11.5			Bits
f_{IN} = 210 MHz	25°C		12.0/12.2		Bits
f_{IN} = 300 MHz	25°C		11.9/12.1		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR) (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		95/93		dBFS
f_{IN} = 140 MHz	25°C		94/95		dBFS
f_{IN} = 170 MHz	25°C	82	93/92		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		93/92		dBFS
f_{IN} = 300 MHz	25°C		93/90		dBFS
SFDR (INCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 97 MHz at −2 dB Full Scale	25°C		97/97		dBFS
f_{IN} = 140 MHz at−2 dB Full Scale	25°C		100/95		dBFS
f_{IN} = 170 MHz at −2 dB Full Scale	25°C		100/100		dBFS
f_{IN} = 210 MHz at −2 dB Full Scale	25°C		93/93		dBFS
f_{IN} = 300 MHz at −2 dB Full Scale	25°C		90/90		dBFS
WORST OTHER (EXCLUDING SECOND AND THIRD HARMONIC DISTORTION)					
f_{IN} = 5 MHz	25°C		98/97		dBFS
f_{IN} = 97 MHz	25°C		97/93		dBFS
f_{IN} = 140 MHz	25°C		97/95		dBFS
f_{IN} = 170 MHz	25°C	88	97/93		dBFS
	Full	82			dBFS
f_{IN} = 210 MHz	25°C		97/95		dBFS
f_{IN} = 300 MHz	25°C		97/95		dBFS

- Can be defined different ways
- Only given as typical
- Only specified at 25C

Statistical Characterization of Resistors



$$\sigma_{\frac{R}{R_N}} = \frac{A_R}{\sqrt{WL}} = \frac{A_R}{\sqrt{A}}$$

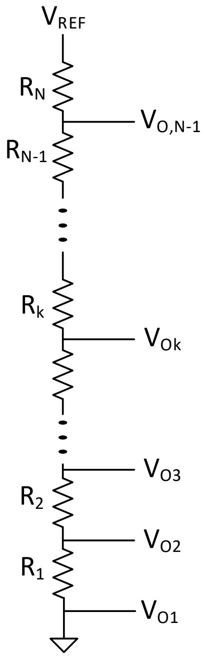
A_R is a process parameter

Note the normalized variance is independent of the resistor value !

Ratio Matching Effects in Data Converters

- Ratio matching is often critical in ADCs and DACs
- Accuracy and matching of gains is also critical in some data converters

String DAC Statistical Performance



Recall $INL_k = V_{OUT}(k) - V_{FIT}(k)$

$$0 \leq k \leq N-1$$

- INL is of considerable interest
- $INL = Max(|INL_k|), \quad 0<k<N-1$
- INL is difficult to characterize analytically so will focus on INL_k

Assume resistors are uncorrelated RVs but identically distributed, typically zero mean Gaussian

String DAC Statistical Performance

It can be shown that INL_k is zero-mean gaussian and

$$\sigma_{INL_k} = \sigma_{\frac{R_R}{R_N}} \sqrt{\frac{(N-k)(k-1)}{N-1}}$$

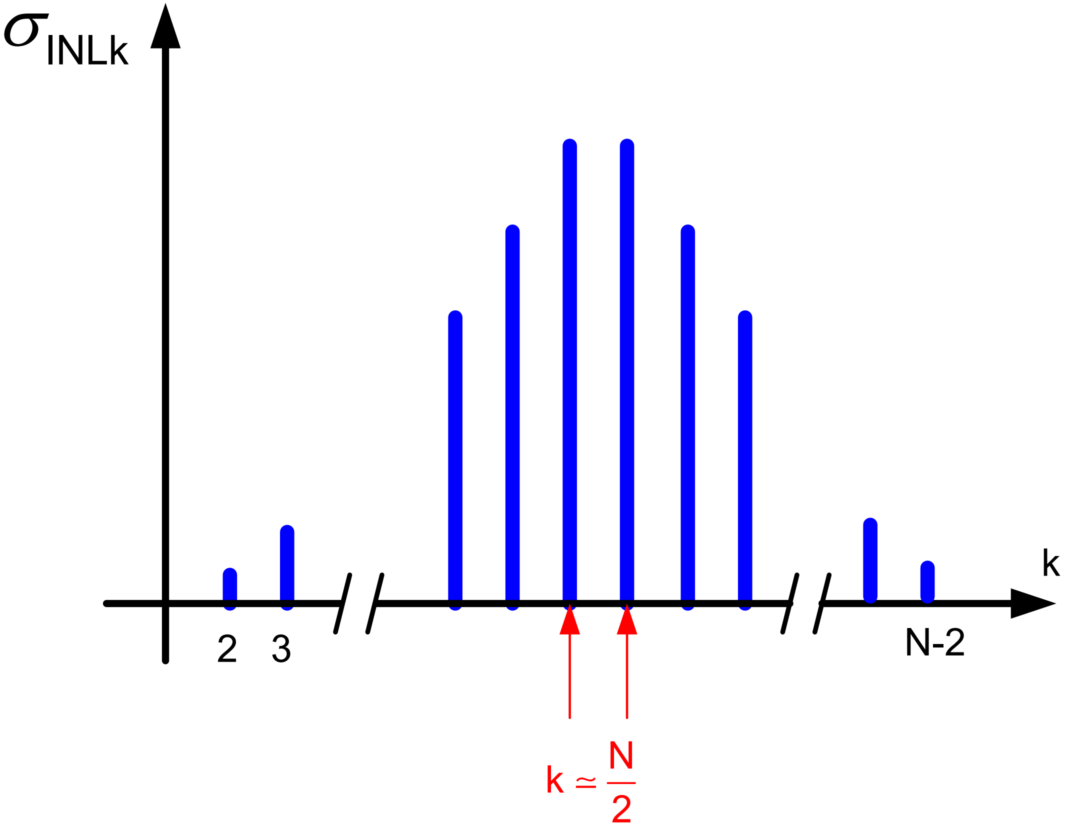
Note this is a nice closed-form expression for the standard deviation of INL_k for a string DAC !!

Observe this assumes a maximum value at about k=N/2

$$\sigma_{INL_k MAX} \simeq \sigma_{\frac{R_R}{R_N}} \sqrt{\frac{\left(N-\frac{N}{2}\right)\left(\frac{N}{2}-1\right)}{N-1}} \simeq \sigma_{\frac{R_R}{R_N}} \frac{\sqrt{N}}{2}$$

String DAC Statistical Performance

standard deviation of INL_k assumes a maximum variance at mid-code

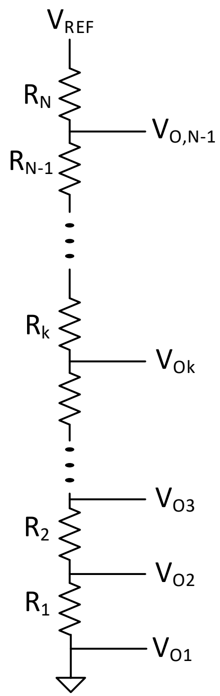


Recall INL_k is Gaussian and

$$\sigma_{INLk\max} = \sigma_{\frac{R_R}{R_{NOM}}} \frac{\sqrt{N}}{2}$$

String DAC Statistical Performance

Example 1:



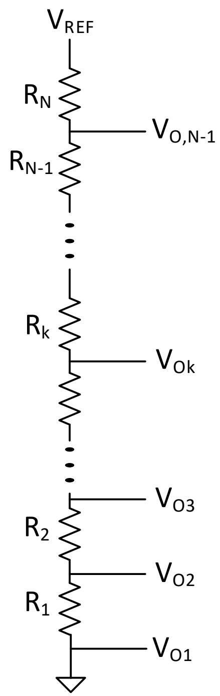
Assume specification for 7-bit String DAC $\left|INL_{kMAX}\right| < 1$ LSB and Pelgrom matching parameter $A_\rho = 0.1$ µm

Desired Yield Y = 99%

Determine the resistor area A to achieve this yield

Example 1:

Determine the resistor area A to achieve this yield



Define $z = INL_{kMAX}$

$$z : N\,(0 \;\; \sigma_z)$$

$$\sigma_z \simeq \sigma_{\frac{R}{R_N}} \bullet \frac{\sqrt{N}}{2}$$

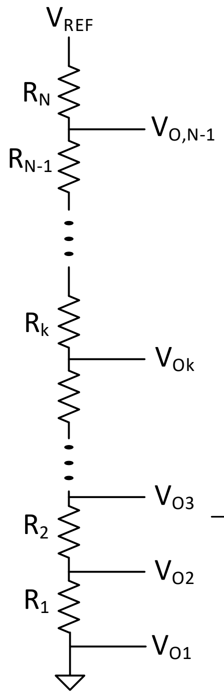
Assume f_z is the PDF of z

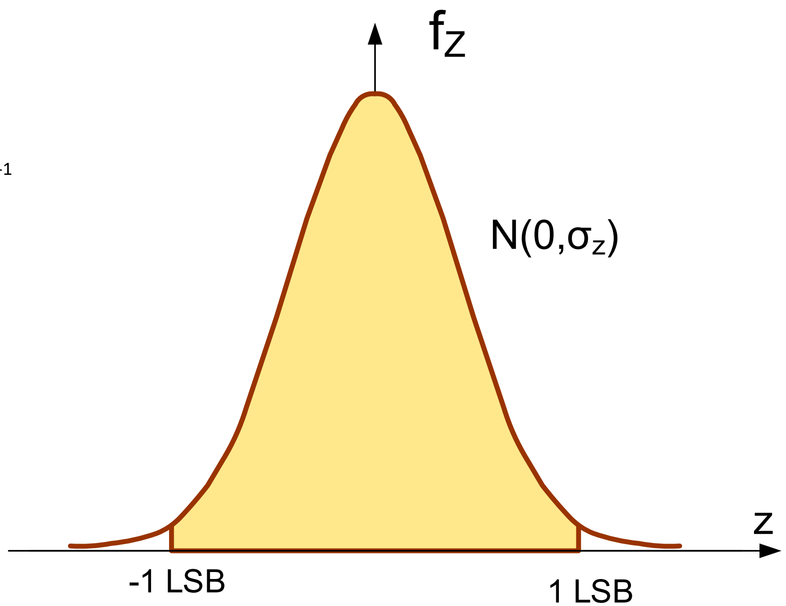
Solution strategy: Obtain σ_z , then solve above equation for $\sigma_{\frac{R}{R_N}}$

and then solve $\sigma_{\frac{R}{R_N}}$ for A : $\sigma_{\frac{R}{R_N}} = \frac{A_R}{\sqrt{WL}} = \frac{A_R}{\sqrt{A}}$

Example 1:

Determine the resistor area A to achieve this yield





Want to determine A so that

$$0.99 = \int_{-1LSB}^{1LSB} f_z(z)\,dz$$

Define: $z_N = \dfrac{z}{\sigma_Z}$ $\qquad z_{N1} = \dfrac{1\,LSB}{\sigma_Z}$

$$z_N \sim N(0,1)$$

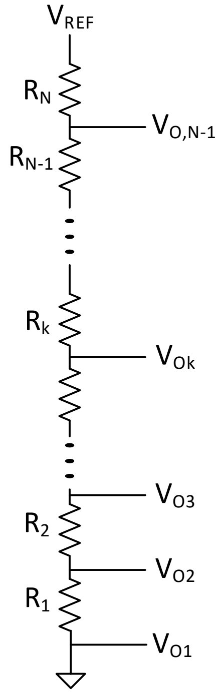
Notation: pdf of z_N is $f_N(z_N)$

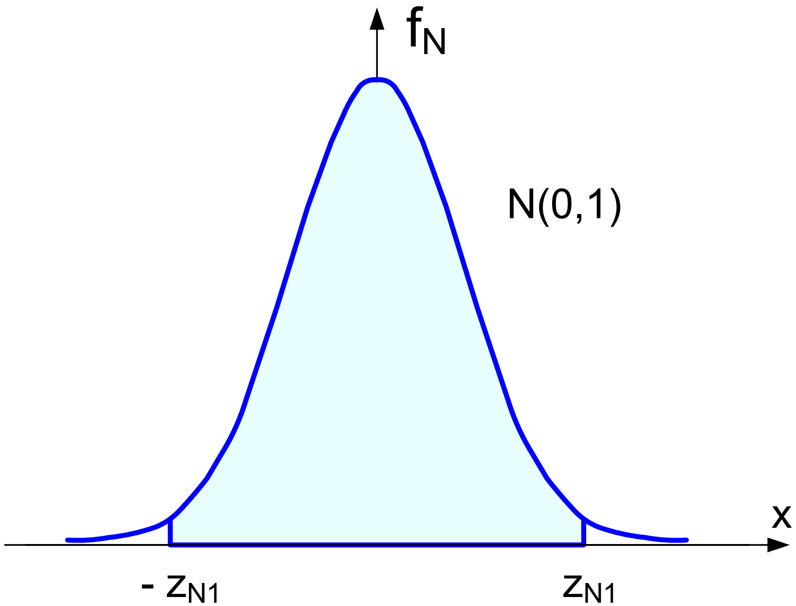
By change of variables, want

$$0.99 = \int_{-Z_{N1}}^{z_{N1}} f_N(z)\,dz$$

Example 1:

Determine the resistor area A to achieve this yield





$$0.99 = \int_{-Z_{N1}}^{Z_{N1}} f_N(z)\,dz$$

$$0.99 = 2F_N(z_{N1}) - 1$$

$$F_N(z_{N1}) = 0.995$$

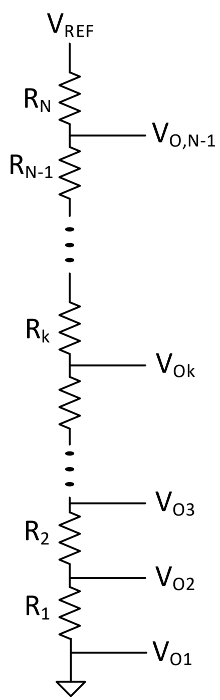
$$F_N\left(z_{N1}\right) = 0.995$$

$$Z_{N1}=2.575$$

z	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
0.2	0.5793	0.5832	0.5871	0.5910	0.5948	0.5987	0.6026	0.6064	0.6103	0.6141
0.3	0.6179	0.6217	0.6255	0.6293	0.6331	0.6368	0.6406	0.6443	0.6480	0.6517
0.4	0.6554	0.6591	0.6628	0.6664	0.6700	0.6736	0.6772	0.6808	0.6844	0.6879
0.5	0.6915	0.6950	0.6985	0.7019	0.7054	0.7088	0.7123	0.7157	0.7190	0.7224
0.6	0.7257	0.7291	0.7324	0.7357	0.7389	0.7422	0.7454	0.7486	0.7517	0.7549
0.7	0.7580	0.7611	0.7642	0.7673	0.7703	0.7734	0.7764	0.7794	0.7823	0.7852
0.8	0.7881	0.7910	0.7939	0.7967	0.7995	0.8023	0.8051	0.8078	0.8106	0.8133
0.9	0.8159	0.8186	0.8212	0.8238	0.8264	0.8289	0.8315	0.8340	0.8365	0.8389
1.0	0.8413	0.8438	0.8461	0.8485	0.8508	0.8531	0.8554	0.8577	0.8599	0.8621
1.1	0.8643	0.8665	0.8686	0.8708	0.8729	0.8749	0.8770	0.8790	0.8810	0.8830
1.2	0.8849	0.8869	0.8888	0.8907	0.8925	0.8944	0.8962	0.8980	0.8997	0.90147
1.3	0.90320	0.90490	0.90658	0.90824	0.90988	0.91149	0.91309	0.91466	0.91621	0.91774
1.4	0.91924	0.92073	0.92220	0.92364	0.92507	0.92647	0.92785	0.92922	0.93056	0.93189
1.5	0.93319	0.93448	0.93574	0.93699	0.93822	0.93943	0.94062	0.94179	0.94295	0.94408
1.6	0.94520	0.94630	0.94738	0.94845	0.94950	0.95053	0.95154	0.95254	0.95352	0.95449
1.7	0.95543	0.95637	0.95728	0.95818	0.95907	0.95994	0.96080	0.96164	0.96246	0.96327
1.8	0.96407	0.96485	0.96562	0.96638	0.96712	0.96784	0.96856	0.96926	0.96995	0.97062
1.9	0.97128	0.97193	0.97257	0.97320	0.97381	0.97441	0.97500	0.97558	0.97615	0.97670
2.0	0.97725	0.97778	0.97831	0.97882	0.97932	0.97982	0.98030	0.98077	0.98124	0.98169
2.1	0.98214	0.98257	0.98300	0.98341	0.98382	0.98422	0.98461	0.98500	0.98537	0.98574
2.2	0.98610	0.98645	0.98679	0.98713	0.98745	0.98778	0.98809	0.98840	0.98870	0.98899
2.3	0.98928	0.98956	0.98983	$0.9^{2}0097$	$0.9^{2}0358$	$0.9^{2}0613$	$0.9^{2}0863$	$0.9^{2}1106$	$0.9^{2}1344$	$0.9^{2}1576$
2.4	$0.9^{2}1802$	$0.9^{2}2024$	$0.9^{2}2240$	$0.9^{2}2451$	$0.9^{2}2656$	$0.9^{2}2857$	$0.9^{2}3053$	$0.9^{2}3244$	$0.9^{2}3431$	$0.9^{2}3613$
2.5	$0.9^{2}3790$	$0.9^{2}3963$	$0.9^{2}4132$	$0.9^{2}4297$	$0.9^{2}4457$	$0.9^{2}4614$	$0.9^{2}4766$	$0.9^{2}4915$	$0.9^{2}5060$	$0.9^{2}5201$
2.6	$0.9^{2}5339$	$0.9^{2}5473$	$0.9^{2}5604$	$0.9^{2}5731$	$0.9^{2}5855$	$0.9^{2}5975$	$0.9^{2}6093$	$0.9^{2}6207$	$0.9^{2}6319$	$0.9^{2}6427$
2.7	$0.9^{2}6533$	$0.9^{2}6636$	$0.9^{2}6736$	$0.9^{2}6833$	$0.9^{2}6928$	$0.9^{2}7020$	$0.9^{2}7110$	$0.9^{2}7197$	$0.9^{2}7282$	$0.9^{2}7365$
2.8	$0.9^{2}7445$	$0.9^{2}7523$	$0.9^{2}7599$	$0.9^{2}7673$	$0.9^{2}7744$	$0.9^{2}7814$	$0.9^{2}7882$	$0.9^{2}7948$	$0.9^{2}8012$	$0.9^{2}8074$
2.9	$0.9^{2}8134$	$0.9^{2}8193$	$0.9^{2}8250$	$0.9^{2}8305$	$0.9^{2}8359$	$0.9^{2}8411$	$0.9^{2}8462$	$0.9^{2}8511$	$0.9^{2}8559$	$0.9^{2}8605$
3.0	$0.9^{2}8650$	$0.9^{2}8694$	$0.9^{2}8736$	$0.9^{2}8777$	$0.9^{2}8817$	$0.9^{2}8856$	$0.9^{2}8893$	$0.9^{2}8930$	$0.9^{2}8965$	$0.9^{2}8999$

Example 1:

Determine the resistor area A to achieve this yield



$$\left.\begin{array}{l} Z_{N1}=2.575 \\ \\ Z_{N1}=\dfrac{1\,\mathrm{LSB}}{\sigma_Z} \end{array}\right\} \Rightarrow \sigma_Z = 0.388$$

but

$$\sigma_Z = \sigma_{\frac{R}{R_N}} \bullet \frac{\sqrt{N}}{2} = \frac{A_\rho}{\sqrt{A}} \bullet \frac{\sqrt{N}}{2}$$

$$0.388 = \frac{A_\rho}{\sqrt{A}} \bullet \frac{\sqrt{N}}{2}$$

$N = 127$ and $A_\rho = 0.1\ \mu m$

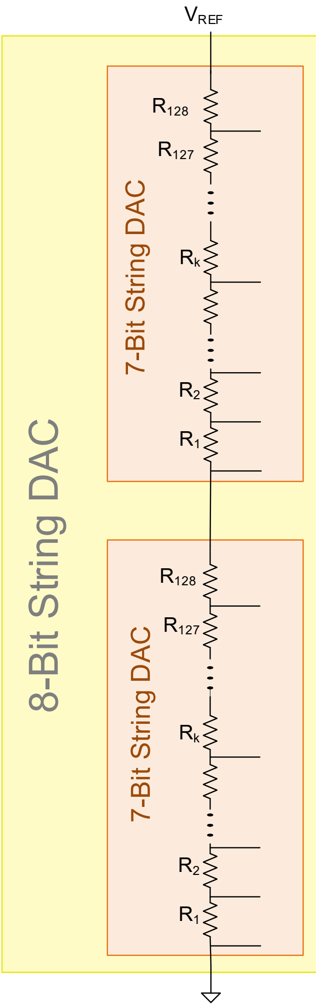
Solving, obtain

$$A = 2.13\ \mu m^2$$

$$\sigma_{\frac{R}{R_N}} = 0.0685$$

Example 2: Consider an 8-bit DAC obtained by combining 2 of the 7-bit DACs

Determine the yield if the specification is still $\left|INL_{kMAX}\right| < 1\,LSB$



Define $z = INL_{kMAX}$

$$\sigma_z = \sigma_{\frac{R}{R_N}} \bullet \frac{\sqrt{N}}{2}$$

Since same resistors are used, $\sigma_{\frac{R}{R_N}} = 0.0685$

$$\sigma_z = 0.0685 \bullet \frac{\sqrt{256}}{2} = 0.5488$$

$$Y = \int_{-1LSB}^{1LSB} f_z(z)\,dz$$

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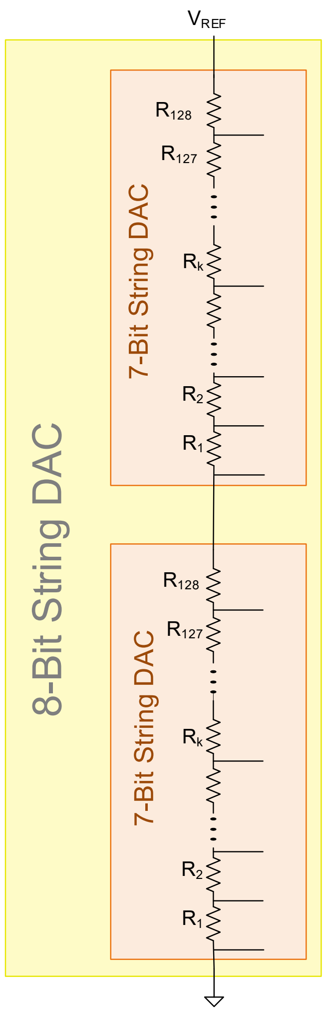
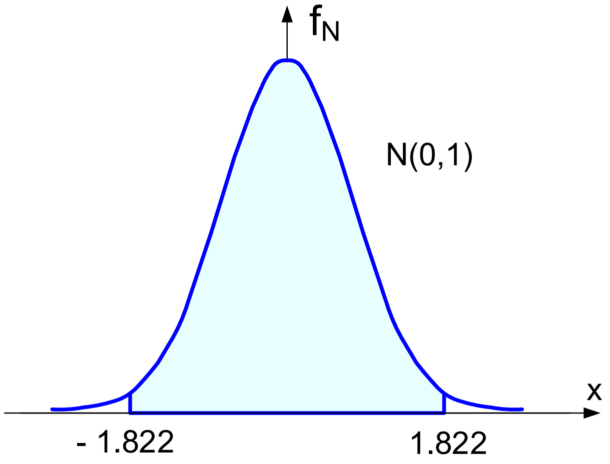


$$Y = \int_{-1LSB}^{1LSB} f_z(z)\,dz$$

Define $$z_N = \frac{z}{\sigma_Z}$$

$$z_N = \frac{1\,LSB}{0.5488} = 1.822$$



$$Y = 2F_N(1.822) - 1$$

$F(0.822) = 0.9656$

z	0.00	0.01	$\boxed{0.02}$	0.03	0.04	0.05	0.06	0.07	0.08	0.09
0.0	0.5000	0.5040	0.5080	0.5120	0.5160	0.5199	0.5239	0.5279	0.5319	0.5359
0.1	0.5398	0.5438	0.5478	0.5517	0.5557	0.5596	0.5636	0.5675	0.5714	0.5753
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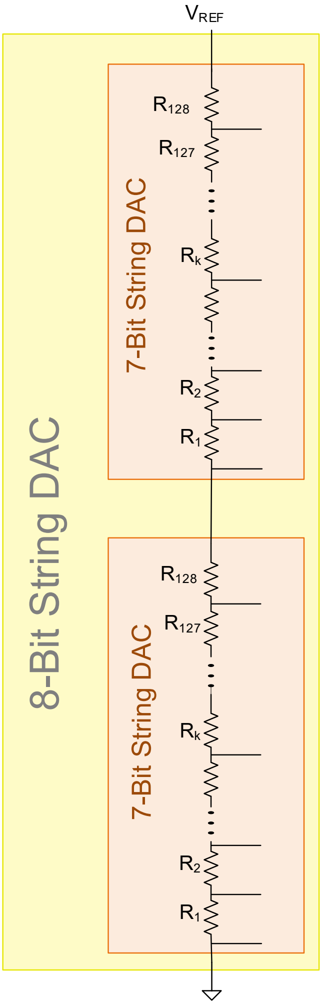
1.4	0.91924	0.92073	0.92220	0.92364	0.92507	0.92647	0.92785	0.92922	0.93056	0.93189
1.5	0.93319	0.93448	0.93574	0.93699	0.93822	0.93943	0.94062	0.94179	0.94295	0.94408
1.6	0.94520	0.94630	0.94738	0.94845	0.94950	0.95053	0.95154	0.95254	0.95352	0.95449
1.7	0.95543	0.95637	0.95728	0.95818	0.95907	0.95994	0.96080	0.96164	0.96246	0.96327
$\boxed{1.8}$	0.96407	0.96485	0.96562	0.96638	0.96712	0.96784	0.96856	0.96926	0.96995	0.97062
1.9	0.97128	0.97193	0.97257	0.97320	0.97381	0.97441	0.97500	0.97558	0.97615	0.97670
2.0	0.97725	0.97778	0.97831	0.97882	0.97932	0.97982	0.98030	0.98077	0.98124	0.98169
2.1	0.98214	0.98257	0.98300	0.98341	0.98382	0.98422	0.98461	0.98500	0.98537	0.98574
2.2	0.98610	0.98645	0.98679	0.98713	0.98745	0.98778	0.98809	0.98840	0.98870	0.98899
2.3	0.98928	0.98956	0.98983	$0.9^2 0097$	$0.9^2 0358$	$0.9^2 0613$	$0.9^2 0863$	$0.9^2 1106$	$0.9^2 1344$	$0.9^2 1576$
2.4	$0.9^2 1802$	$0.9^2 2024$	$0.9^2 2240$	$0.9^2 2451$	$0.9^2 2656$	$0.9^2 2857$	$0.9^2 3053$	$0.9^2 3244$	$0.9^2 3431$	$0.9^2 3613$
2.5	$0.9^2 3790$	$0.9^2 3963$	$0.9^2 4132$	$0.9^2 4297$	$0.9^2 4457$	$0.9^2 4614$	$0.9^2 4766$	$0.9^2 4915$	$0.9^2 5060$	$0.9^2 5201$
2.6	$0.9^2 5339$	$0.9^2 5473$	$0.9^2 5604$	$0.9^2 5731$	$0.9^2 5855$	$0.9^2 5975$	$0.9^2 6093$	$0.9^2 6207$	$0.9^2 6319$	$0.9^2 6427$
2.7	$0.9^2 6533$	$0.9^2 6636$	$0.9^2 6736$	$0.9^2 6833$	$0.9^2 6928$	$0.9^2 7020$	$0.9^2 7110$	$0.9^2 7197$	$0.9^2 7282$	$0.9^2 7365$
2.8	$0.9^2 7445$	$0.9^2 7523$	$0.9^2 7599$	$0.9^2 7673$	$0.9^2 7744$	$0.9^2 7814$	$0.9^2 7882$	$0.9^2 7948$	$0.9^2 8012$	$0.9^2 8074$
2.9	$0.9^2 8134$	$0.9^2 8193$	$0.9^2 8250$	$0.9^2 8305$	$0.9^2 8359$	$0.9^2 8411$	$0.9^2 8462$	$0.9^2 8511$	$0.9^2 8559$	$0.9^2 8605$
3.0	$0.9^2 8650$	$0.9^2 8694$	$0.9^2 8736$	$0.9^2 8777$	$0.9^2 8817$	$0.9^2 8856$	$0.9^2 8893$	$0.9^2 8930$	$0.9^2 8965$	$0.9^2 8999$

Example 2:

Consider an 8-bit DAC obtained by combining 2 of the 7-bit DACs

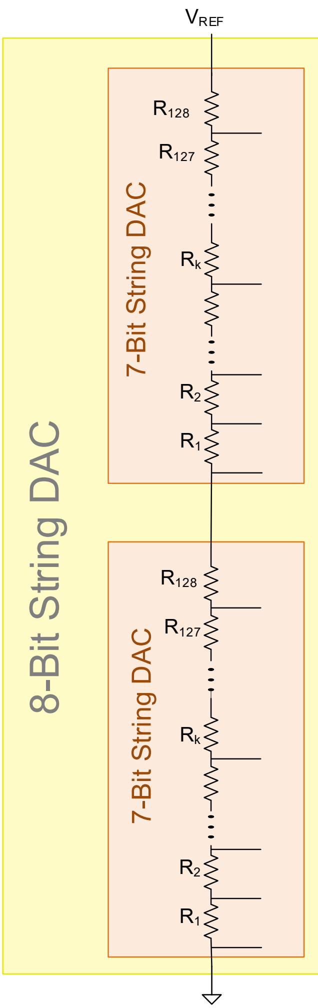


$$Y = 2F_N(1.822) - 1$$

$$Y = 2 \bullet 0.965 - 1 = 0.93$$

Yield has dropped from 99% to 93%

Example 3: What area is needed for obtaining a 99% yield for an 8-bit string DAC and how does that compare to the area required for a 7-bit DAC with the same yield?



For 99% yield

$$\sigma_z = \sigma_{\frac{R}{R_N}} \bullet \frac{\sqrt{N}}{2} = \frac{A_\rho}{\sqrt{A}} \bullet \frac{\sqrt{N}}{2} = 0.388$$

$$\frac{A_\rho}{\sqrt{A}} \bullet \frac{\sqrt{N}}{2} = 0.388$$

$$A_\rho = 0.1\mu m \qquad N = 256$$

$$A = 4.25\,\mu m^2$$

Area doubled because there are twice as many resistors and each is approximately twice as big so by adding 1-bit of resolution, the area went up by approximately a factor of 4

String DAC Statistical Performance

How about statistics for the INL?

$$\mathrm{INL} = \max_{1<k<N} \left|\mathrm{INL}_k\right|$$

$$\mathrm{INL}_k = \frac{1}{R_{NOM}}\left[\sum_{j=1}^{k} R_{Rj}\left(1-\frac{k}{N-1}\right)-\frac{k}{N-1}\sum_{j=k+1}^{N-1} R_{Rj}\right] \qquad 1 \le k \le N-1$$

- INL is an <u>order statistic</u>
- Distribution functions for order statistics are very complicated and closed form solutions do not exist !
- INL is not zero-mean and not Gaussian
- Statistical simulations using Monte-Carlo analysis often used to predict INL yield but these simulations can be extremely time consuming if the order of the data converter is very large

How important is statistical analysis?

- Statistical analysis of data converters is critical
- Some architectures are more sensitive than others to statistical variations in components
- The onset of yield loss due to statistical limitations is generally quite abrupt and can have disastrous effects if not considered as part of the design process

  Recall examples where σ_{VOS}=5mV compared with σ_{VOS}=1mV

- Substantially over-designing to avoid concerns about statistical yield loss is not a practical solution since the area penalty, the speed penalty, and the power penalty are generally quite severe

For the effects of local random variations of a parameter X, generally

$$\sigma_X \propto \frac{A_0}{\sqrt{A_C}}$$

where A_C is the area of the matching critical components and A_0 is a process parameter

Stay Safe and Stay Healthy !

End of Lecture 38